c. 3

SANDIA REPORT

SAND97–0155 • UC–706
Unlimited Release
Printed January 1997

Modular Weapon Control Unit

Michael F. Boccabella, Gary N. McGovney

Prepared by
Sandia National Laboratories
Albuquerque, New Mexico 87185 and Livermore, California 94550
for the United States Department of Energy
under Contract DE-AC04-94AL85000

SF2900Q(8-81)

Issued by Sandia National Laboratories, operated for the United States Department of Energy by Sandia Corporation.

Available to DOE and DOE contractors from
Office of Scientific and Technical Information
PO Box 62
Oak Ridge, TN 37831

Prices available from (615) 576-8401, FTS 626-8401

Available to the public from
National Technical Information Service
US Department of Commerce
5285 Port Royal Rd
Springfield, VA 22161

NTIS price codes
Printed copy: A03
Microfiche copy: A01

SAND97 – 0155
Unlimited Release
Printed January 1997

Distribution
Category UC–706

Modular Weapon Control Unit

Michael F. Boccabella
Real-Time Monitors & Controllers Department

Gary N. McGovney
Power Electronics & Custom Controllers Department
Sandia National Laboratories
Albuquerque, NM 87185-0537

Abstract

The goal of the Modular Weapon Control Unit (MWCU) program was to design and develop a reconfigurable weapon controller (programmer/sequencer) that can be adapted to different weapon systems based on the particular requirements for that system. Programmers from previous systems are conceptually the same and perform similar tasks. Because of this commonality and the amount of re-engineering necessary with the advent of every new design, the idea of a modular, adaptable system has emerged. Also, the controller can be used in more than one application for a specific weapon system. Functionality has been divided into a Processor Module (PM) and an Input/Output Module (IOM). The PM will handle all operations that require calculations, memory, and timing. The IOM will handle interfaces to the rest of the system, input level shifting, output drive capability, and detection of interrupt conditions. Configuration flexibility is achieved in two ways. First, the operation of the PM is determined by a surface mount Read-Only Memory (ROM). Other surface-mount components can be added or neglected as necessary for functionality. Second, IOMs consist of configurable input buffers, configurable output drivers, and configurable interrupt generation. Further, these modules can be added singly or in groups to a Processor Module to achieve the required I/O configuration. The culmination of this LDRD was the building of both Processor Module and Input/Output Module. The MWCU was chosen as a test system to evaluate Low-Temperature Co-fired Ceramic (LTCC) technology, desirable for high component density and good thermal characteristics.

Acknowledgments

Because of the large time lag between the completion of the LDRD and the departure of the principle investigator, individual persons will not be acknowledged. The groups responsible for the success of various aspects of this project are: Sandia National Laboratories (SNL) Department 2337 for Electrical and Mechanical Engineering; SNL Department 2335 for advanced packaging concepts, specifically LTCC; SNL Department 2274 for digital Application Specific Integrated Circuit (ASIC) design; SNL Department 2272 for analog ASIC design; SNL Department 2411 for fabrication design and support; and Allied Signal/Kansas City Division for process design and manufacturing.

Preface

This preface is to explain the circumstances surrounding this Sand report. The principle investigator, Mike Boccabella, left Sandia National Laboratories late in 1993. Unfortunately he left before writing a Sand report. This was left undiscovered until late 1996 when Gary McGovney was asked to prepare this report. Mr. Boccabella had reached the point in the LDRD of having received manufactured units of both the Processor Module and the Input/Output Module. At the time of his leaving, the interest in modular controller design had grown beyond Mr. Boccabella's LDRD to a project which outlived several funding project terminations. This was the Modular Adaptable Controller (MAC) project, at that time known as the Modular Adaptable Control Module (MACM) project. Department resources were devoted to the development of the MAC modules for several customers. Mr. Boccabella's LDRD had produced demonstrable hardware and was seen as more than achieving its intended goal. As the initial designer of the MAC Central Processing Unit (CPU) Module, his work directly carried over into the MAC project. Mr. McGovney completed the final design stages of the MAC CPU Module; and, although having no involvement with the MWCU LDRD, was chosen as the most knowledgeable about Mr. Boccabella's work. The documents that comprise this report have been gathered from the few remaining files three years after the project's completion, but they do contain complete specifications for the PM and IOM design requirements, project goals, and photographs of the completed units. The latter portion of this preface will briefly discuss the MAC module project.

The MAC project shared a similar design philosophy with the MWCU. The functionality of a programmer was divided into five groups. The groups are: Processing, Input, Output, Use Control Interface, and Power Regulation. The Power Regulation had two planned modules: Linear Regulation and Switching Regulation. The CPU Module contains an 8051 microprocessor, address decoder, reset & initialization circuitry, two UARTs, five timers, five I/O ports, an interrupt handler, up to 32kbytes of EEPROM, and a controllable clock IC. The Input Module has eight buffers, eight comparators, and two differential comparators. All of these inputs are level detect configurable. The Output Module has eight high-current drivers which are configurable as high or low side drivers and can operate in switch or current limit mode. The Linear Power module had planned +15V, +5V, and –5V power supplies, power-on reset circuit, low-power drive, and selectable current limiting. The Switching Power Module had planned DC-DC conversion providing reliable output voltages above battery voltage. The Use Control Module had planned interface circuitry for CAP and MET, and power supplies to drive both CAP and MET. The Power Regulation and Use Control Modules have built ASICs but have not built working modules for several reasons, the most notable of which is funding cuts for the project. The CPU, Input, and Output Modules have all been used in a demonstration programmer for the Advanced Electrical System Architecture (AESA) Bus Demonstration Project. Planned future uses for the MAC Module family are currently on hold pending funding.

Contents

Figures

Modular Weapon Control Unit

1.1 Introduction

The goal of the Modular Weapon Control Unit (MWCU) program is to design and develop a reconfigurable weapon controller (programmer/ sequencer) that can be adapted to different weapon systems based on the particular requirements for that system. Programmers from previous systems are conceptually the same and perform similar tasks. Because of this commonality and the amount of re-engineering necessary with the advent of every new design, the idea of a modular, adaptable, system has emerged. Also, the controller can be used in more than one application for a specific weapon system. The MWCU will be able to function as a WCU, an ICU, nuclear surety device, or function in ground based equipment for pre-flight programming.

While this modular system must be backward compatible with previous designs so that Stockpile Improvement initiatives can be satisfied, it must also be forward looking to anticipate designs that are not yet considered. From the standpoint of backward compatibility, design is a matter of covering all specifications from previous systems. Forward looking designs however are more difficult because specifications for these systems have not yet been generated. The requirements discussed in the following sections will detail the capabilities of the MWCU for use in future applications.

Modularity for this device is achieved through the use of surface mount devices. A surface mount Read Only Memory (ROM) will provide the personality to determine the task the module is to perform. This personality module will contain instructions for how the controller is to behave and will have the rules that associate input signals with their corresponding output signals. Other surface mount devices will be attached to the unit depending on the needs of the particular application. The concept of modularity is extended to other areas of this system as well. All Software and Mechanical engineering are based on modular approaches. Modular software will permit reliable and fast prototype development of ROM's for testing particular applications. Modular mechanical engineering will provide several different configurations for the system. These configurations can be used to fit the system into a wide variety of space constraints imposed by mechanical requirements for various systems.

1.2 Organizational Matrix

This project involves several organizations at Sandia National Labs, as well as Allied Signal/Kansas City Division. Department 2337 is responsible for the Electrical and Mechanical Engineering for the MWCU. Department 2335 is working in the area of advanced packaging concepts for the MWCU. Specifically, Low Temperature Co-Fired Ceramic is being used for packaging. Department 2274 is concerned with Digital Application Specific Integrated Circuit (ASIC) design. ASIC's are used to reduce the amount of chips needed to implement a design. Typically, the processor and its associated support logic will be implemented using a digital ASIC. Department 2272 will design an analog ASIC for use in the input output driver circuits. Department 2411 will provide design and fabrication support for the advanced packaging. The packaging medium is Low Temperature Co-fired Ceramic. A multichip module will be designed and built in support of the electrical design of Department 2337 and the packaging design of Department 2335. Allied Signal/Kansas City Division (AS/KCD) will perform final assembly of the module. Assembly will entail mounting bare dies on the surface of the ceramic module and hermetically sealing the module. Also, it is necessary to surface mount devices on the outside of the package. The work performed by AS/KCD is in direct support for process development initiatives at AS/KCD. Their effort and the SNL effort are working in parallel to bring both facilities on line for design and fabrication of Low Temperature Co-Fired Ceramic Multichip Modules.

1.3 Prototype Evaluation

Background investigation for this project is currently underway. The B90 Weapon Control Unit was chosen as a test system to evaluate the technology of Low Temperature Cofired Ceramic. This system was selected because an ASIC version of the microprocessor was already developed, as well as the fact that the testers are still available as AS/KCD. The existence of the testers will make evaluation of the system easier, as the results of the B90 programmer can be compared directly with the results of the newly packaged B90 programmer. Functionally, this module will be identical to the B90 ASIC based Weapon Control Unit.

1.4 System Overview

The MWCU is comprised of two types of modules. One module, the processor module, will perform all processing and decision making functions. This module will handle all initialization and power detection tasks. Input power will be closely monitored by this device to ensure the modules have the proper voltage levels for correct operation. Rise time, built-in self tests, and boundary scan (JTAG) techniques will be available for further confidence in proper operation. Modularity on the processor module is achieved by changing the surface mount ROM. The processor will obtain its operating characteristics from the program that is stored in ROM.

Changing the ROM will allow the module to be redefined to solve a different problem. Standardized signal levels and loads will be used for communications with I/O modules. Also, a standard pin out will be used so the processor can be connected to one or more I/O modules.

A second module, the Input/Output module, will perform signal conditioning, level shifting, and communication formatting tasks. Different drivers will be available on this module for different situations. Digital inputs and outputs as well as high current digital outputs will be provided. An analog input and output will be provided. Serial communications from the processor module will be translated here to industry standard RS232/422 levels. Circuit modules will be designed so that customized I/O modules can be fabricated quickly to match the specific requirements for a project. A designer can look in a library of circuit modules and select the number of each type of I/O required. Design of a custom I/O module is then a matter of laying out the pre-designed circuits, fabricating the ceramic modules, and assembling the units.

Software libraries will be generated to operate the different electrical devices available. The modular hardware/software approach will make testing easier since specific portions of the hardware can be tested by invoking specific portions of the software libraries. This will tend to isolate small portions of the software and hardware for debugging purposes.

Both types of modules will be interconnected with a mechanical fixture that will provide flexible packaging options. A mechanical block diagram of the processor module and two I/O modules is shown in Fig. 1. A functional block diagram of the system is shown in Fig. 2.

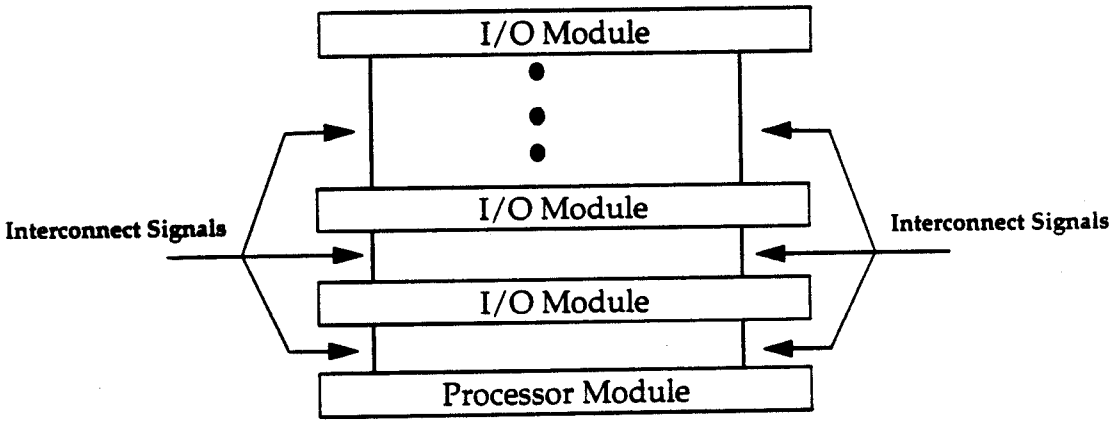


Figure 1. Mechanical Block Diagram

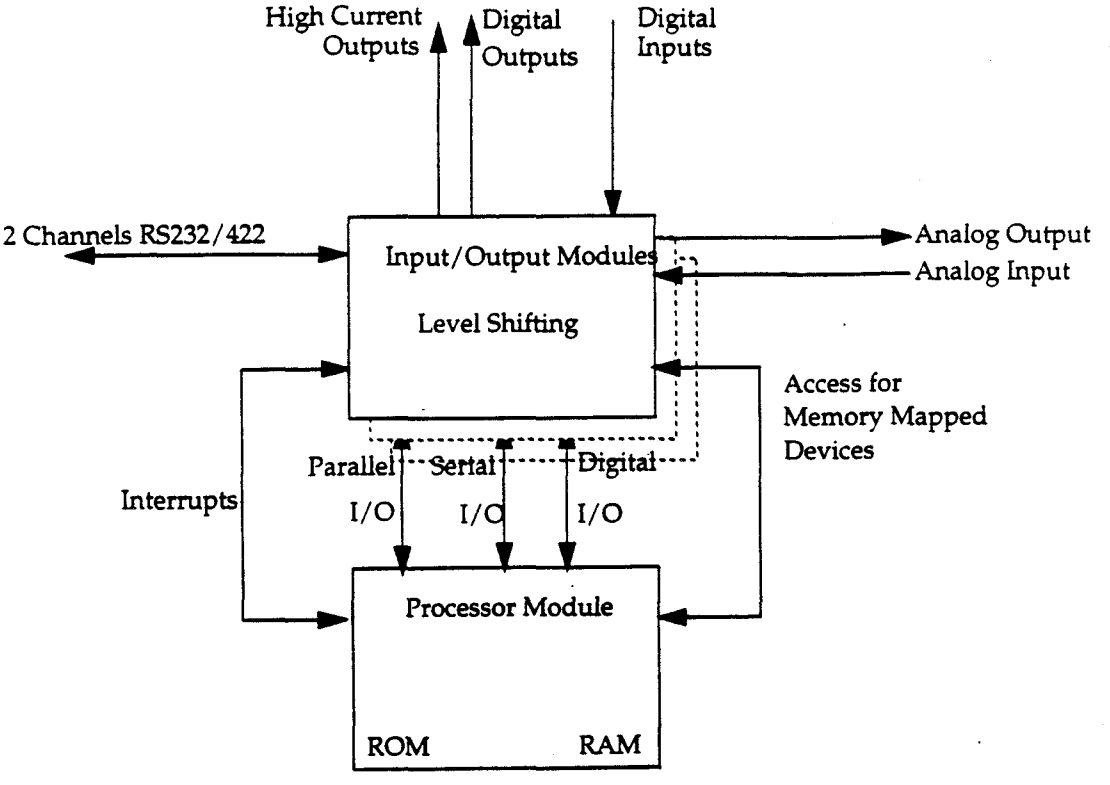


Figure 2. Functional Block Diagram

1.5 Definition of Terms

Active Low: A signal that is asserted when it is in its low state.

Active High: A signal that is asserted when it is in its high state.

TTL signal: A signal which conforms to industry standard levels generated by TTL logic chips. A low signal is defined as any signal less than 0.7 Volts DC. A high signal is defined as any signal greater than 3.0 Volts DC. Any signal outside of this range is said to be undefined.

Rising Edge: The edge encountered when changing from TTL Low to TTL High.

Falling Edge: The edge encountered when changing from TTL High to TTL Low.

ASIC: Application Specific Integrated Circuit. A device which replaces conventional discrete logic and high level chips with a single integrated circuit.

WCU: Weapon Control Unit.

ICU: Interface Control Unit.

Interrupt Vectors: A fixed location in memory where the processor looks to determine what section of code to execute. A portion of the system memory is reserved as the vector table. Every device and situation that can cause an interrupt has a location in the table.

Bus Cycle: Time necessary to complete one operation on the data bus. This will be a minimum of one system clock.

System Clock: The master clock that operates the system. This will be the reference for all timing information.

RAM: Random Access Memory is memory that be read from and written to. This type of memory is typically used by software to store results from calculations.

ROM: Read Only Memory is memory that can only be read. A write to a ROM device will have no effect. ROM is typically used to store data that will not change (such as software).

NVRAM: Non-Volatile RAM is RAM that will retain data even after power has been removed. This type of memory is also called EEPROM.

EEPROM: Electrically Erasable Programmable Read Only Memory is memory that can be erased by the microprocessor, and rewritten. The device will retain data even after power has been removed. This type of memory is also called NVRAM.

1.6 Document Control

Control of this document remains with Department 2337 (Real Time Monitors and Controls). Initial release, and subsequent changes to this document require the approval of Department 2337.

Processor Module Functional Requirements

2.1 Processor Module Description

The processor module will perform all timing and decision making tasks necessary for the operation of the MWCU. Inputs to the MWCU are accepted via the I/O Module and routed to the processor module so decisions can be generated. The decisions, in conjunction with timing information are used to generate outputs. Capabilities of the processor module include 5 internal programmable timers, 2 Serial Communication channels, 1 parallel channel, 48 channels of programmable discrete digital input/output lines, and decoding for memory mapped devices that are mounted on the I/O module. Examples of memory mapped devices include, A/D convertors, D/A convertors, communications interfaces such as MIL-STD 1553, and expandable I/O devices. Memory mapped modules will have interrupt capabilities available. Each of the 48 programmable I/O lines has its own interrupt priority. Line 47 has the highest priority, and line 0 the lowest among the I/O lines.

Testability and manufacturability issues will be addressed through concurrent engineering, process characterization, and Quality Function Deployment (QFD). Testability will be enhanced with the capability of boundary scan (JTAG) built into the processor module. Test vectors can be passed through the system and the output analyzed with diagnostic routines. Manufacuturability is addressed through the involvement of production agencies early in the design process. Evaluation of a prototype programmer (B90) is underway which will provide information about Low Temperature Cofired Ceramic as well as uncover fabrication and assembly problems that may be encountered during the development of the Modular Weapon Control Unit.

2.2 Specifications

Following is a description of the capabilities for each part of the processor module of the MWCU. Individual portions of the entire module are considered. A block diagram of the Processor Module is presented in Fig. 3.

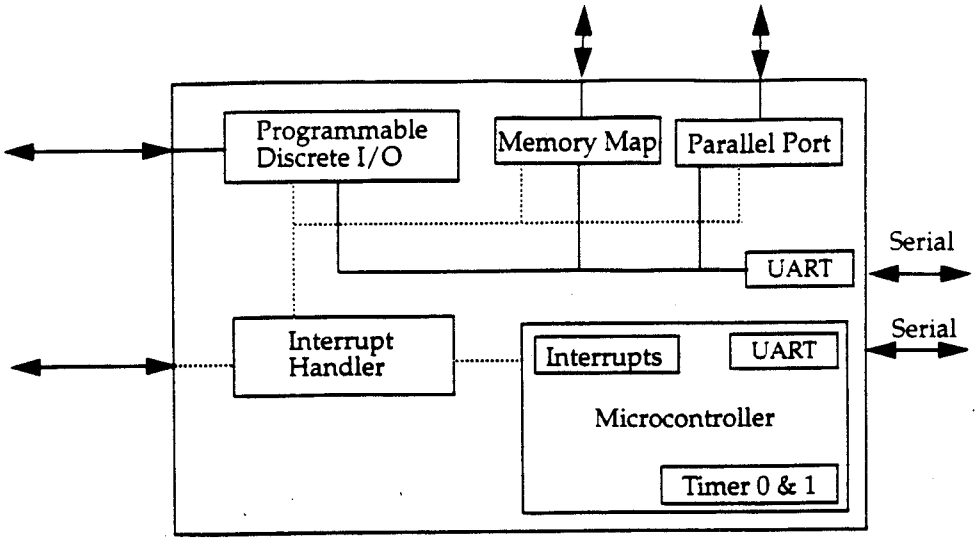


Figure 3. Processor Module

2.2.1 System Power Up

It is imperative to maintain control of the state of all output signals while the circuit is undergoing varying power conditions. Spikes and dips in the input supply power will not be seen at the processor or any of its outputs. If the supply voltage stays within the selected range, the processor will not be interrupted. At power up, the module will detect a user selectable voltage at which point the system will begin operation. Voltage selection is performed through the use of external resistors surface mounted to the package. The range of acceptable voltages is 12 Volts through 24 Volts. When the voltage detect circuit determines input power has been applied, all devices on the MWCU are reset. User adjustable hysteresis will be used to determine when power has been interrupted. Voltage detect will be independent of the rise time of the input supply. Infinite rise time (step input) through slow rise time signals will be acceptable. Even a noisy input supply (due to supply loading) can be tolerated provided the thresholds are not exceeded. See Fig. 4 for a pictorial description. Hysteresis is set by the difference between the On Threshold and the Off Threshold.

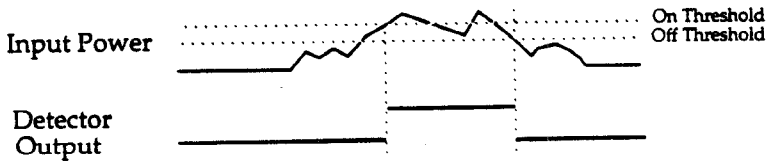


Figure 4. Voltage Detection

2.2.2 Input Voltage Range

Maximum input voltage to the processor module is limited to 36 Volts DC. Any voltage above the selected voltage detect, and below 36 Volts DC, will place the processor module in an operational state. Operation above 36 Volts may cause permanent damage.

2.2.3 System Reset

When a system reset occurs, all devices with state memory are held in a reset state for 250 milliseconds. Reset will allow the processor module to begin operation in a known state. Inputs are disregarded during reset, and outputs are held in a low state during reset. As the reset period ends, the processor resident in the processor module will begin execution at the code pointed to by the reset vector pointer. Start up code for the processor must first enable the outputs by sending the proper sequence of data to unlock the outputs. If the processor does not send the correct sequence, the outputs will remain in an inhibited state. If the correct code is sent, the outputs are enabled and the user code can continue executing. See Fig. 5 for a diagram of system reset.

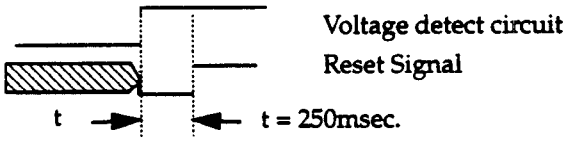


Figure 5. Reset Timing

2.2.4 Internal Programmable Timers

Five internal timers are present on the processor module. These timers can be used for generating output pulses with programmable width, measuring the width of an input pulse, or measuring the time between two different signals. The timers are controlled and loaded through the processor. Timers can be set to generate interrupts upon time-out. Each serial port used will require one timer to generate its baud rate.

Two timers (T0 & T1) are contained in the 80C51. Access to these timers is as discussed in the Intel 8-Bit Microcontroller Data Book. Three additional timers (T2, T3 &T4) are available via the 82C54 internal to the ASIC. These timers are accessed through MOVX instructions to external memory locations. The 82C54 requires four addresses to operate. One address is an overall configuration register (control word register), and the other three are the counter registers for each timer. Refer to the Intel Peripheral Devices Data Book for specific details about the 82C54.

Additionally, each timer in the 82C54 has a programmable divider cascaded in front of it. This divider serves a pre-scaler to divide the incoming frequency by 1 to 256. A configuration register and counter register are

necessary for each programmable divider. The counter register is an 8-bit register used to set the count of the programmable divider. The configuration register will select the input frequency to the programmable divider (SYS_CLK, SYS_CLK/8), gate for counting, and whether that timer can generate an interrupt. The IE bit will enable interrupts (IE=1 is enabled, IE=0, disabled). The Gate bit is used to control the operation of the counter and the programmable divider(Gate=1 will enable counting, Gate=0 disables counting). The F/S bit will select the fast or slow oscillator source for the counter (F/S=1 counts at OSC rate, F/S=0 counts at OSC/8 rate). Time limits on the 82C54 timers are 1μs < T < 11.185 seconds, assuming a 12 MHz SYS_CLK. Longer timers can be obtained with slower system clocks.

If the 8251A UART is used, T4 will provide the baud rate generation. This is the only timer that can be u[illegible] to generate the baud rate.

2.2.5 Serial Communication Channels

Two channels of serial communication are available. All communication on the processor module is at TTL voltage levels. Level shifting to RS232/422 compatible signals will be done on the I/O module. Both channels will support full duplex operation. The baud rate for communication is programmable from 300 bits per second to 19.2K bits per second. Both channels can generate interrupts upon reception and transmission of information. Data format is selectable as defined by RS232/422 standards. There is choice of 7 or 8 data bits, zero or one stop bits, and even/odd/no parity. Commands and data can be sent to the MWCU via the serial port. Data can be stored directly in any portion of RAM (see Fig. 6) depending on the interrupt routine associated with the serial channel.

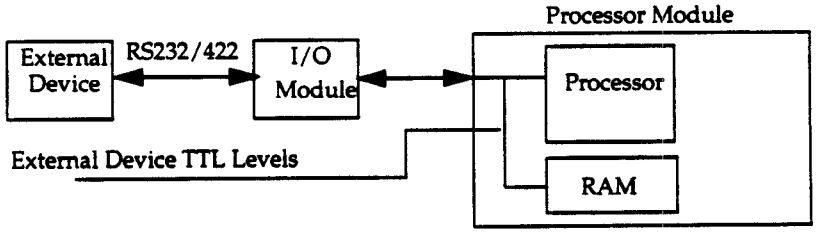


Figure 6. Serial Communications

2.2.6 Parallel Communication Channel

One parallel port is provided. This is a bidirectional port that will accept input and generate output at TTL levels. Interrupt support is provided upon reception of new data. Data can be transferred (written) to this port from an external source by placing the data on the data lines, and strobing the data-in latch line. A rising edge on the data-in strobe will latch in the data and generate the interrupt if interrupts are enabled. Data must be

valid for 100 nanoseconds before the rising edge to ensure proper transfer. The processor can likewise write data to the port by placing data on the data lines and strobing the data-out line. A rising edge on the data-out latch line will indicate to external devices that data is available. The processor module and all external devices must manage the direction of the port. Collisions between incoming and outgoing data should be avoided. As with the serial channel, commands and data can be read directly in from the parallel port and stored in memory. One word of data can be transferred at a time, and the bandwidth of data transfer will be limited by the interrupt routine that is servicing the parallel port. A minimum of 2 memory reads will be necessary for one word of transfer. See Fig. 7for a diagram of timing for parallel communications over the data bus.

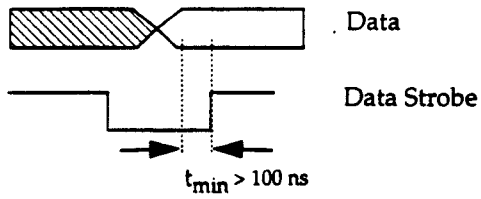


Figure 7. Parallel Communications

2.2.7 Memory Mapped Devices

Memory Mapped devices may be built into the I/O Module. Address decoding is done on the processor module. Each memory mapped device will have a base address defined by the memory map. All other memory locations are relative to the base. Each device will have access to sixteen unique memory locations. Data size for each word of data is eight bits. Up to four memory mapped devices may be designed into the I/O units. Memory access is done according to Fig. 8. Select lines are mutually exclusive lines that will select at most, one external memory mapped device per bus cycle. The four bit address bus will select one of the (up to) sixteen memory locations of the external device. Data will then be placed on the eight bit data bus. All signals shown in Fig. 8 are generated by the processor module, and propagated to the I/O module for connection to the external device. Timing for memory mapped access is shown in Fig. 9. For a write, the processor will place the data on the data bus, select the address to use and place it on the address bus, and a write will occur. The address will generate the select line as well as the 4 bit address. The write occurs on the rising edge of the next clock pulse. For a read, the processor will place the address onto the address bus, and data will be available on the rising edge of the next clock pulse. A maximum access time for any external device is 250nSec.

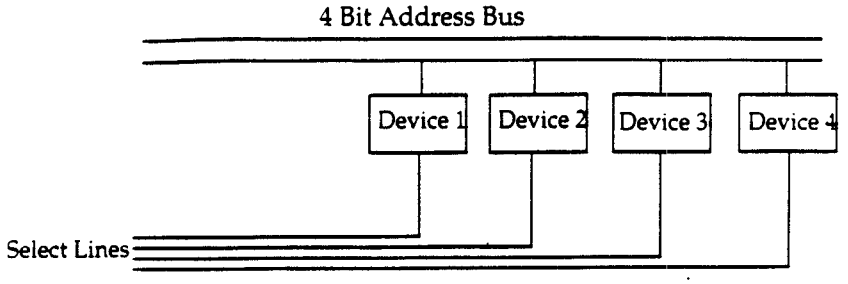


Figure 8. Block Diagram of Memory Mapped Devices.

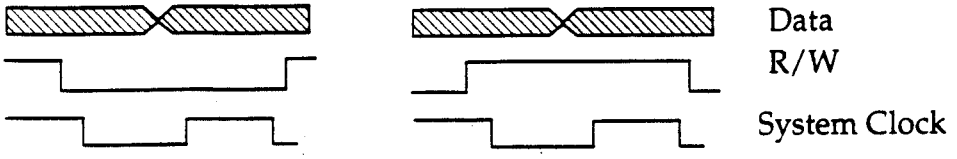


Figure .A Reading Data Figure .B Writing Data

Figure 9. Accessing Memory Mapped Devices

Typically, A/D and D/A convertors as well as non-volatile RAM are good candidates for memory mapped devices. Also, communication channels such as MIL-STD 1553 could be implemented through this capability if the application requires it.

2.2.8 Discrete Input/Output Channels

Discrete I/O is one of the most important features of the MWCU. Decisions made by the processor are based in the 48 programmable input/output channels. Each channel can be programmed as an input or an output. Interrupt service is available for the inputs. Interrupts can be generated based on transitions (rising or falling edges) on the input channels, or they can be selected as level sensitive. The internal counters/timers can be used to time the distance between transitions on two different channels, or they can measure the pulse width of a single channel. Interrupt processing initiated by the discrete I/O channels will be important for detecting the occurrence of interesting events.

Each channel can be programmed to be an input or an output, however the circuitry in the I/O module must match that. Therefore, there is a hardware dependency on the signal direction based on the circuit in the I/O module. See Fig. 10 for a diagram. To reduce the complexity of the circuitry, discrete I/O lines must be programmed in blocks of 4 lines. For example, I/O 47

through I/O 44 must all be identical (input or output, level or edge triggered, and, low or high level).

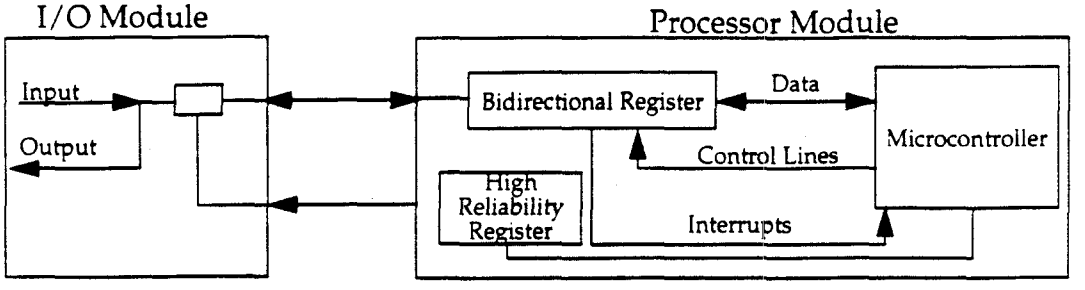


Figure 10. Discrete I/O Channels

2.2.9 High Reliability Outputs

Four outputs are provided on the processor module that can be used for increased reliability on critical signals. These lines are provided to prevent a single device failure from generating an output. The processor must enable the high-rel output, and then the signal can be enabled. The signal will only become true when both outputs are enabled. Logically this function can be thought of as an AND gate where both signals are necessary to generate an output. Typically, series transistors will be used for implementation though. Use of the high reliability outputs is shown in Fig. 10.

2.3 Interrupt Processing

Interrupt processing is a vital and necessary component for a controller. Each I/O line will have its own priority level. I/O 47 has the highest priority of the I/O lines, and the priority decreases down until I/O 0 has the lowest. Other support functions (serial port, memory mapped devices etc.) also have interrupt capability. The entire interrupt priority structure is shown in Fig. 11 in order of decreasing priority. The 80C31 microcontroller is limited to 2 external interrupts. All external devices (I/O lines, additional serial, and additional timers) must be mapped into these two interrupts. This is handled through a priority encoder that can prioritize at most two external events. Use of an example will serve to illustrate the point. If I/O 0 generate an interrupt, it will be serviced. If, during the interrupt routine, I/O 1 generates an interrupt, I/O 0 will be suspended in order to service I/O 1. If I/O 2 then generates an interrupt, it will not be serviced until I/O 1 is completed. This limitation is imposed by the two level structure of the 80C31.

Device	Priority
Timer 0 **	2/59

Device	Priority
I/O 47	58
...	
I/O 0	11
Serial 1 Rcv	10
Serial 1 Tx	9
Timer 4	8
Timer 3	7
Timer 2	6
Mem Map 3	5
Mem Map 2	4
Mem Map 1	3
Mem Map 0	2
Timer 0 **	2/59
Timer 1	1
Serial 0 R/T	0

Figure 11. Interrupt Priorities for MWCU devices

Timer 0 is internal to the 80C31, and its interrupt priority falls between the two levels of external interrupts. If the processor is servicing an external interrupt, and timer 0 generates an external interrupt, the processor will suspend the external interrupt and take care of timer 0. If the processor is already servicing two interrupts as in the example above, the timer will not be serviced until the high priority external interrupt is completed.

2.4 Interconnect Signals between Processor and I/O Module

All signals passing between the I/O Module and the Processor Module will be TTL compatible voltage levels.

A signal generated by the processor module will be in the following range:

High State $2.4 < V_{OH} < 5.0$ Volts

Low State $0.0 < V_{OL} < 0.7$ Volts

The current handling/drive capabilities for the output drive circuit of the processor module will be in the following range:

$$I_{OH} < 4 \text{ mA}$$

$$I_{OL} < 4 \text{ mA}$$

A signal received by the processor module will be interpreted according to the following relations:

High State $2.4 < V_{IH} < 5.0$ Volts

Low State $0.0 < V_{IL} < 0.7$ Volts

The current drive necessary for all incoming signals is will be in the following range:

$$I_{IH} < 10\mu A$$

$$I_{IL} < 10\mu A$$

Since the capability for more than one I/O module exists, it is the responsibility of the designer to ensure that the load limits are not exceeded. The processor module will supply a maximum of 4 mA for each signal. All I/O modules connected to the processor must draw less than the 4 mA available. This will limit the number of I/O modules that may be connected to a processor module. Any additional current requirements must be provided by the addition of buffering on custom I/O modules that are designed.

2.5 Memory Capacity

Random Access Memory (RAM) will be available for use by the software. This memory is used for data storage during execution. Calculations completed during execution can be placed in RAM for later use. The user will have 256 bytes of RAM for program store. Note, this space includes the system stack and all local variables. Another type of RAM will also be available, but it can't be used as general read/write memory. This memory is called Non-Volatile RAM (NVRAM). It has very slow write times, and can only be written in blocks of 64 Bytes. NVRAM can be used to store data while the system is powered down. The user will have 8K bytes of NVRAM.

ROM will be used for storing the program (software) to execute. Program store will be 8K bytes. The memory map for the system is shown in Fig. 12.

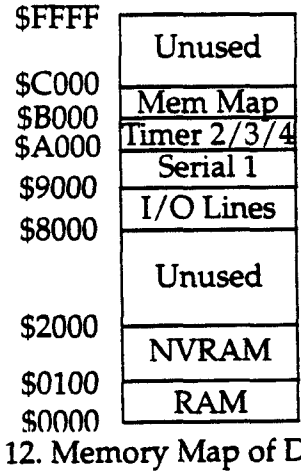


Figure 12. Memory Map of Data Area

Processor Module Testing

3.1 General Description

Typically, testing of a system or subsystem is driven by a set of requirements to ensure that the unit is functioning as expected. When testing a generic device though, it is important to test functionality of the individual pieces that make up the unit instead of the entire unit. System or subsystem testing to a set of requirements will be done when an application is identified, and the functionality of the unit is described by requirements.

Testing for the processor module will be limited to testing the power up sequence, functionality of interrupt routines developed for each type of device on the processor module, and use of memory mapped devices. For example, the interrupt handler for the programmable I/O lines must be tested to ensure that it is responding to the correct type of input, and only the correct type of input.

3.2 Signal Definition

Signals needed to drive the inputs are:

Rising Edge:	Transition from 0 to 5 Volts
Falling Edge:	Transition from 5 to 0 Volts
High Level:	5 Volts
Low Level:	0 Volts
High Pulse:	5 Volts for 250μsec
Low Pulse:	0 Volts for 250μsec

A maximum of 10μA will be needed to drive any single input.

Outputs from the processor module will be in the range as described in Sec. 2.4.

3.3 Voltage Detect Test: #1

The purpose of this test is to determine at what point the voltage detect circuit will generate a system reset (t_0). For this test, the signal V_DET_OVD must be tied to ground through a jumper on the test assembly. Main Battery power will be ramped from 0 to 28 Volts in 28msec (1 Volt/msec). System reset will be generated when the battery voltage passes the predetermined set voltage. Two surface mount resistors are used to set this point. Once 28 volts is reached, the battery voltage will be reduced to 0 Volts at the same rate. When the input voltage reaches it cutoff point, system reset will be removed. The cutoff voltage is set by an external surface

mount resistor. See Fig. 13 for a diagram of the battery voltage and system reset functions. Signals to be recorded are battery voltage, and system reset.

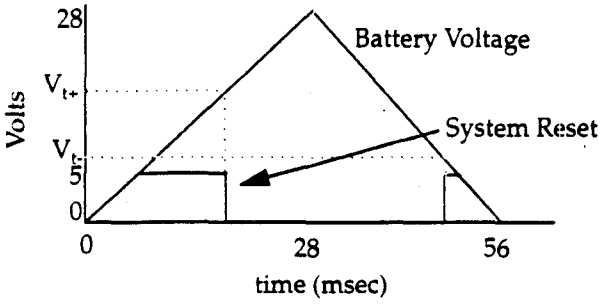


Figure 13. System Reset Function with Internal +5 Volts

3.4 Voltage Detect Test: #2

This test will check for proper operation of the voltage detect override circuitry. For this test, the signal V_DET_OVD must be allowed to float. The external LM117 regulator must be removed from the socket, and an external 5 Volt supply connected to the +5 Volt input to the processor module. In this situation, main battery and pulse battery will not influence the generation of the system reset signal. The thick film resistor and surface mount capacitor will provide an RC time constant to allow the oscillator to begin operation. Fig. 14 shows the signal V_DET_OVD, and system reset. At t_0, +5 Volts is applied to the processor module. Curves in Fig. 14 are calculated based on the model LSI Logic provided for their input schmitt trigger inverter. Signals to be measured are V_DET_OVD and SYS_RST.

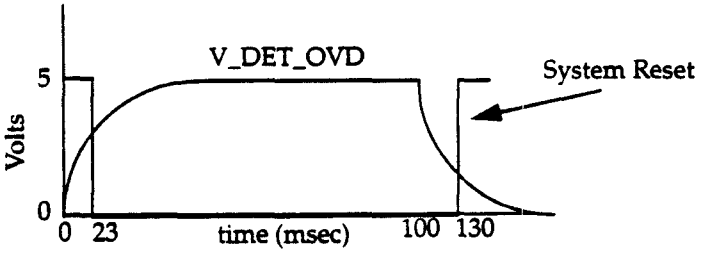


Figure 14. System Reset Function with External +5 Volts

3.5 Processor Module Configuration: Test #3

The processor module has 48 programmable I/O lines. In this test, each line will be tested as an input and an output. At the beginning of the test, the processor module software will configure line 0-23 as inputs, and 24-47 as outputs. Each input line will control one output line. When a stimulus is applied to line 0, line 24 will generate a high level output. All 24 inputs will be arranged this way. All four possible methods of stimulation will be tested on each line. When the first 24 I/O lines are tested as input, and the other 24 tested as output, their roles will be reversed. Lines 0-23 will be

outputs, and lines 24-47 are inputs. Each of the inputs will again be tested, and their corresponding output observed. The matrix for Test #1 is shown in Fig. 15.

Input Lines	Input Signal	Associated Outputs	Expected Output	Activation Time (sec)	Testing
0 thru 47	Undetermined	Undetermined	Low Level	0 thru 1	
0 thru 23	High Level	24 thru 47	Low Level	1 thru 1.5	
0 thru 23	Low Level	24 thru 47	High Level	1.5 thru 2	Falling Edge
0 thru 23	High Level	24 thru 47	High Level	2 thru 2.5	
0 thru 23	Low Level	24 thru 47	Low Level	3 thru 3.5	
0 thru 23	High Level	24 thru 47	High Level	3.5 thru 4	Rising Edge
0 thru 23	Low Level	24 thru 47	High Level	4 thru 4.5	
0 thru 23	High Level	24 thru 47	Low Level	5 thru 5.5	
0 thru 23	Low Pulse	24 thru 47	Oscillate	5.5 thru 6	Low Level
0 thru 23	High Level	24 thru 47	Last State	6 thru 6.5	
0 thru 23	Low Level	24 thru 47	Low Level	7 thru 7.5	
0 thru 23	High Pulse	24 thru 47	Oscillate	7.5 thru 8	High Level
0 thru 23	Low Level	24 thru 47	Last State	8 thru 8.5	
24 thru 47	High Level	0 thru 23	Low Level	10 thru 10.5	
24 thru 47	Low Level	0 thru 23	High Level	10.5 thru 11	Falling Edge
24 thru 47	High Level	0 thru 23	High Level	11 thru 11.5	
24 thru 47	Low Level	0 thru 23	Low Level	12 thru 12.5	
24 thru 47	High Level	0 thru 23	High Level	12.5 thru 13	Rising Edge

Input Lines	Input Signal	Associated Outputs	Expected Output	Activation Time (sec)	Testing
24 thru 47	Low Level	0 thru 23	High Level	13 thru 13.5	
24 thru 47	High Level	0 thru 23	Low Level	14 thru 14.5	
24 thru 47	Low Pulse	0 thru 23	Oscillate	14.5 thru 15	Low Level
24 thru 47	High Level	0 thru 23	Last State	15 thru 15.5	
24 thru 47	Low Level	0 thru 23	Low Level	16 thru 16.5	
24 thru 47	High Pulse	0 thru 23	Oscillate	16.5 thru 17	High Level
24 thru 47	Low Level	0 thru 23	Last State	17 thru 17.5	

Figure 15. Matrix for Test #3.

The matrix in Fig. 15 will test each I/O line for proper operation and generation of interrupts. Each line will be tested with all possible interrupt sources, and only the correct source should generate an interrupt. Each line can trigger off of a rising edge, falling edge, high level, or low level. Each group of 3 lines in the matrix will test all four conditions. The output should only change state when the proper source is presented to the I/O line.

In each step of the test, 24 lines are being tested. To facilitate this, the inputs will be sequenced through in 10 ms intervals as shown in Fig. 16. It will take 0.24 sec to sequence through all 24 lines.

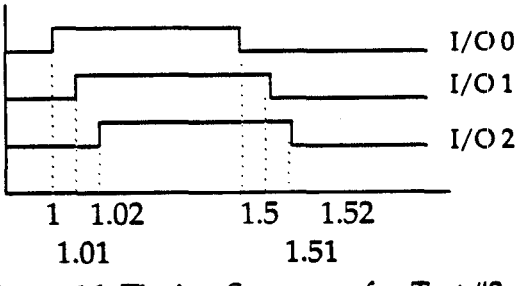


Figure 16. Timing Sequence for Test #3

3.6 Processor Module Configuration: Test #4

This test will check the interrupt handler for multiple interrupts occurring at the same time. Three inputs will be fired simultaneously. Each will be connected to a different input, thus a different priority. Peripheral devices will also be tested for interrupt handling. A timer will be set to expire at the

same time an input arrives. This will test the handling of interrupts generated from two different types of devices. Serial ports will receive data, and at the end of each character, will assert an output. Also, it will echo the character on its transmit side. Each timer will be exercised, and instructed to generate an interrupt at the roughly the same time. The matrix for test 2 is shown in Fig. 17. Note, in Fig. 17 lines 47,46&45 are all changed simultaneously, not on 10msec intervals as in the previous test.

Inputs	Activation	Associated Outputs	Output	Activation Time(sec)
0 thru 47	Undetermined	Undetermined	Low Level	0 thru 1.0
47	Rising Edge	0	High Level	1.0
46	Rising Edge	1	High Level	1.0
45	Rising Edge	2	High Level	1.0
41	Rising Edge	3	High Level	2.0
42	Rising Edge	4	High Pulse	2.000005
43	Rising Edge	5	High Level	2.000010
44	Rising Edge	6	High Pulse	2.000015
Timer 2	Internal	7	High Level	3.0
40	Rising Edge	8	High Level	3.0
Serial 0 Rx Data	9600 Baud Data	9 Parallel Port Serial 0 Txd	High Level Character Character	4.0 4.0 4.0
Serial 1 Rx Data	9600 Baud Data	2 Parallel Port Serial1 Txd	High Level Character Character	5.0 5.0 5.0
Timer 0	Internal	10	High Level	6.0
Timer 1	Internal	11	High Level	6.0

Inputs	Activation	Associated Outputs	Output	Activation Time(sec)
Timer 2	Internal	12	High Level	6.0
Timer 3	Internal	13	High Level	6.0
Timer 4	Internal	14	High Level	6.0

Figure 17. Matrix for Test #4

3.7 Processor Module Configuration: Test #5

Test #3 will check for proper operation of the Memory Mapped lines and the high reliability output lines. Inputs will be sent to the processor, and they will be used to generate outputs. Four inputs will directly control the high reliability lines. When the input line is activated, the processor module will activate the associated high reliability output. Four inputs will directly control the memory mapped select lines. When the input line is activated, the processor module will activate the associated memory mapped select output.

Inputs	Activation	Associated Outputs	Output	Activation Time(sec)
0 thru 47	Undetermined	Undetermined	Low Level	0 thru 1.0
47	Rising Edge	HR0	High Level	1.00
46	Rising Edge	HR1	High Level	1.01
45	Rising Edge	HR2	High Level	1.02
44	Rising Edge	HR3	High Level	1.03
SEL0	Rising Edge	INT0	Low Level	1.10
SEL1	Rising Edge	INT1	Low Level	1.11
SEL2	Rising Edge	INT2	Low Level	1.12
SEL3	Rising Edge	INT3	Low Level	1.13

Figure 18. Matrix for Test #5

Input/Output Module Functional Requirements

4.1 I/O Module Description

The I/O module described here is intended to be a general purpose module that can be used in many applications. It may be necessary to design a specialized module based on the specific requirements of the application. There may not be enough channels of a specific type to suit individual requirements, but any modular circuit contained in this module can be used as is in an application specific design.

Discrete I/O is the most important aspect of the MWCU. The processor module permits the direction of the discrete signal to be programmable, however the I/O module must define which direction the signal will be. This definition is necessary so the correct level shifting can be done on the input signals. Therefore, this I/O module has defined that 16 of the 48 discrete channels will be used. The remaining 32 I/O lines will be unused, and can be occupied by other I/O modules defined at a later date. Of the 16 lines used, 8 will be dedicated as inputs, and 8 will be outputs.

Testability and manufacturability issues will be addressed through concurrent engineering and process characterization. Testability will be enhanced through the use of modular circuits. Specifically, manufacuturability is addressed through the involvement of production agencies early in the design process.

4.2 Specifications

Following is a description of the requirements for each part of the I/O module. Individual portions of the entire module are considered. A block diagram of the I/O Module is presented in Fig. 19.

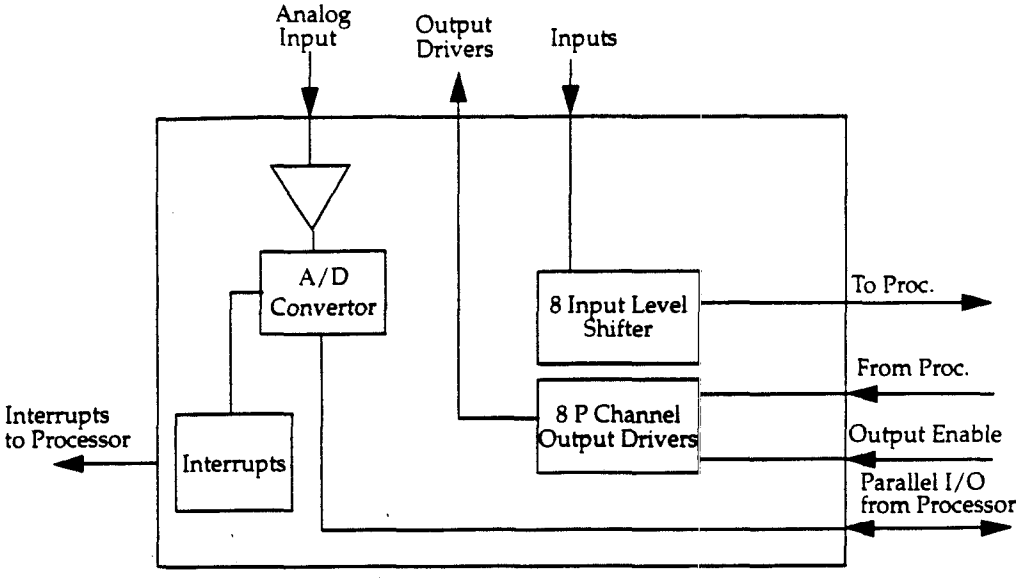


Figure 19. I/O Module

4.2.1 System Power Up

System power up is a time that requires tight control on the state of inputs and outputs. The processor module will control the state of the outputs during this time. All outputs from the processor module will be in a logic low state until the processor changes them. Also, enable lines from the processor module will be in a low state until the processor enable the outputs. The processor module will ignore all inputs until power up is completed. System Reset is available as an input to this module to reset any resident devices.

4.2.2 Discrete Inputs

Eight of the 48 discrete I/O lines have been dedicated as inputs on this module. The voltage level at which they will cause a trigger to the processor module is user selectable via surface mount resistors. Inputs to the I/O module must be high impedance, with a maximum input current of 100μA. All trigger levels will be in the range of $5 < t < 36$ Volts. A complete definition of interconnect signals between the processor module and the I/O module is discussed in "Interconnect Signals between Processor and I/O Module" on page 14.

4.2.3 Discrete Outputs

Eight of the 48 discrete I/O lines have been dedicated as outputs on this module. Each of the outputs will be identical in function, but will have different drive capability. Each channel will control a P channel power HEXFET device (SA3483/IRFF9130). Additionally, the output lines will be disabled via output enable lines as shown in Fig. 20. Two output enable

lines will control all eight output drivers. The output must be able to drive the gate of a HEXFET power transistor (100µA max). If the output (from the processor) is low (<0.7V), the output of the I/O module will be high impedance (drain of an off P-Channel device). When the input goes high (>2.0V), the output will be 28 volts supplied through a pass transistor.

Drive capability for the outputs are:

2 Outputs	28V	250ma	Steady State
4 Outputs	28V	5 A	20mSeconds Duration
2 Outputs	28V	2.5A	Steady State

All outputs will be in a high impedance state until the processor module enables the outputs via the output enable lines. Two enable lines will be used to control all eight outputs. Each line will enable 4 of the outputs. See Fig. 20 for details.

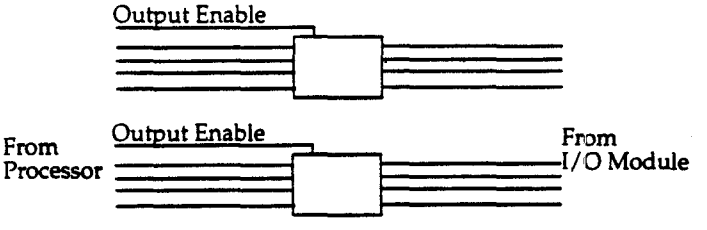


Figure 20. Output line and Output Enables

Output enables will be generated by the processor module after the module has been reset and initialized. This output will be initialized to a '0' at power up, and will change to a '1' when the processor enables that set of outputs. Signal levels for these signals are defined in "Interconnect Signals between Processor and I/O Module" on page 14.

4.2.4 Analog to Digital Convertor

An 8 bit analog to digital convertor is provided on the I/O module as a memory mapped device. The input to the A/D is passed through a linear amplifier for buffering and scaling. External resistors can be used to set the gain of the amplifier. Input to the amplifier should be in the range $0<V_{in}<36V$. Maximum current draw of the scaling amplifier is 100µA. The output of the amplifier will be a maximum of 5 Volts. An interrupt register is available to enable interrupts for the A/D convertor. Interrupt upon completion of a conversion is the only case that can generate an interrupt for the A/D convertor. Maximum conversion time is 5µs, and maximum Icc=20mA. The A/D converter must operate from a single 5 Volt supply.

4.3 Interrupt Processing

The only device on this I/O module that can generate an interrupt is the A/D convertor. As interrupts are generated by this device, they will be passed to the processor module for scheduling and service. An interrupt

configuration register is available on the processor module for enabling and disabling interrupts.

4.4 Module Power

Power applied to the module is unconditioned thermal battery power. The range of battery power is $14<V_{power}<36$ Volts.

4.5 Analog ASIC

The analog ASIC on this module will provide the following functions:

1. Level Shift inputs. The input levels will be in the range as stated above, and the output must be 'low' when the input is below the threshold, and 'high' when the input is above the threshold. Rise time of signals should be $t_{rise} < 1\mu s$, and propagation delay should be $t_{prop} < 1\mu s$.
2. Driver for P-channel power MOSFET. When the signal generated by the processor is 'low', the output should be in a high impedance state so the MOSFET being driven will not turn on. When the processor generates a 'high' level, the output must go 'low' to allow the external P-channel device to turn on. The P-channel device this will control is IRFF9130 (SA3483).
3. A linear amplifier is required to amplify/attenuate the input to an A/D converter. The input to the amplifier is in the range as stated above, and the output must be a linear amplification of that signal with a full scale range of $0<V_{out}<5$ Volts. External resistors will be used to set the gain.
4. The ASIC will generate the following regulated voltages: +12V, +5V, and +2.5V. The +5 Volt regulator must be able to supply 20mA of current to devices external to the ASIC. The +12V and +2.5V outputs are monitor outputs only with a maximum of 1mA of current draw.

Subsystem Capabilities

5.1 Interconnection

Interconnection of a processor module and an I/O module will lead to a system with 8 discrete input channels, and 8 discrete output channels. This system can have any input voltage in the range of 5 to 32 volts, and the outputs will be 28 volt switched outputs. Other capabilities are discussed in previous sections. Interconnection of the two modules is shown in block diagram form in Fig. 21.

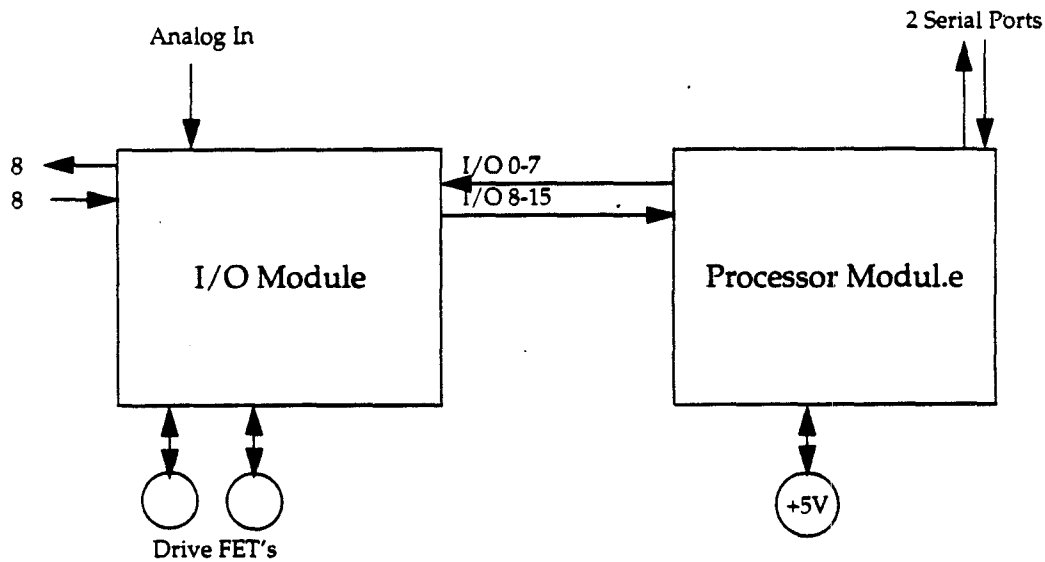


Figure 21. Block Diagram of Module Interconnections

5.2 Capabilities

The limiting feature of this design is the density of the level shifting circuitry and the power handling capability of the I/O module. Functionally, the processor module can be programmed to implement any of the following programmers: B61-3/4, B61-7, B61-9,10, B83, B90, and MAST. Eight inputs and outputs will not permit complete implementation of any specific programmer. Additionally, a large effort would be required to design software to implement the entire function of any programmer. Instead, a subset of functionality has been selected. Typical input levels and output loads/duty cycles were selected from the range of programmers above. If the needed number of output drivers for a specific programmer are connected to the processor module, and the software is written, the programmer function can be performed.

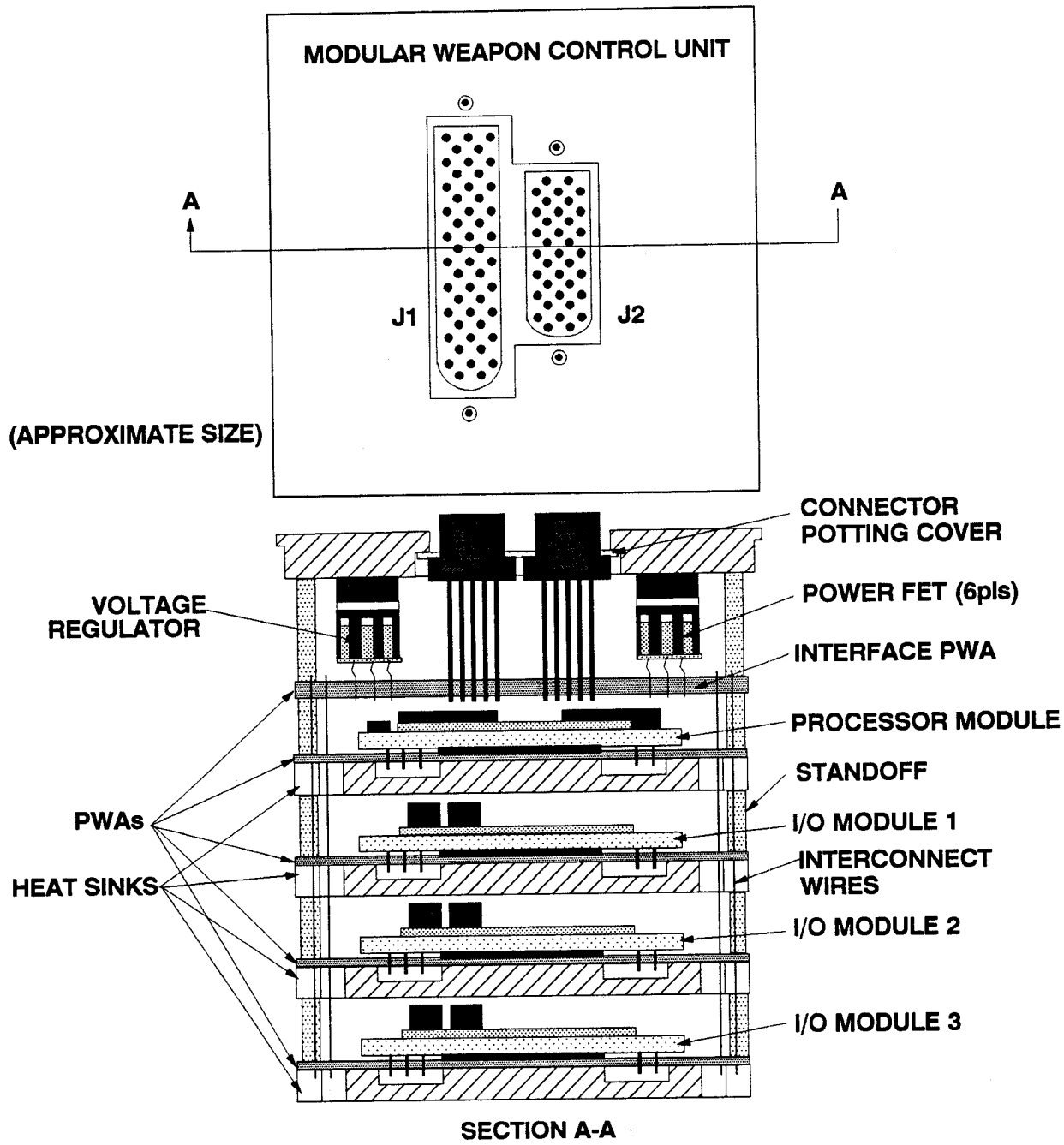
5.3 Limitations

Limitations for this subsystem is the number of I/O lines that can be handled on a single module. Also, as more lines are added to a single module, the less general the module becomes. One main effort of this project is to generate a component that is general in nature. If a large number of I/O lines are dedicated to one unit, only a limited number would be available for future, yet undesigned units. For I/O modules to be compatible, they must each use different processor lines. Only 48 I/O lines are available on the processor module, and each I/O module must use distinct I/O lines to avoid conflicting with another module that may be in the system.

5.4 Future Enhancement

Two major areas with the potential for future development are user selectable I/O lines, and high power handling capability for I/O modules. User selectable I/O lines would eliminate the possibility of conflicting modules in one subsystem. It is impossible to predict the needs of future systems. Since needs cannot be predicted, the I/O module described here is only a projection of what will be needed. If the I/O lines in this module could be assigned to the processor I/O lines by the user, any potential for conflict would be eliminated.
Currently, work is being done in the area of high power dissipation fo driver circuits. The I/O module described here should be compatible (with only minor modifications) with this work.

MODULAR WEAPON CONTROL UNIT
(MWCU)



MWCU CAPABILITY

INPUT LINES -- 20	OUTPUT 250mA -- 6
OUTPUT PULSED 5A -- 12	A-D CONVERTER -- 1
OUTPUT 3A -- 6	RADAR RANGE LINES -- 3

DRK 1/18/94 SMWCU

Figure 22. MWCU Concept Drawing 1.

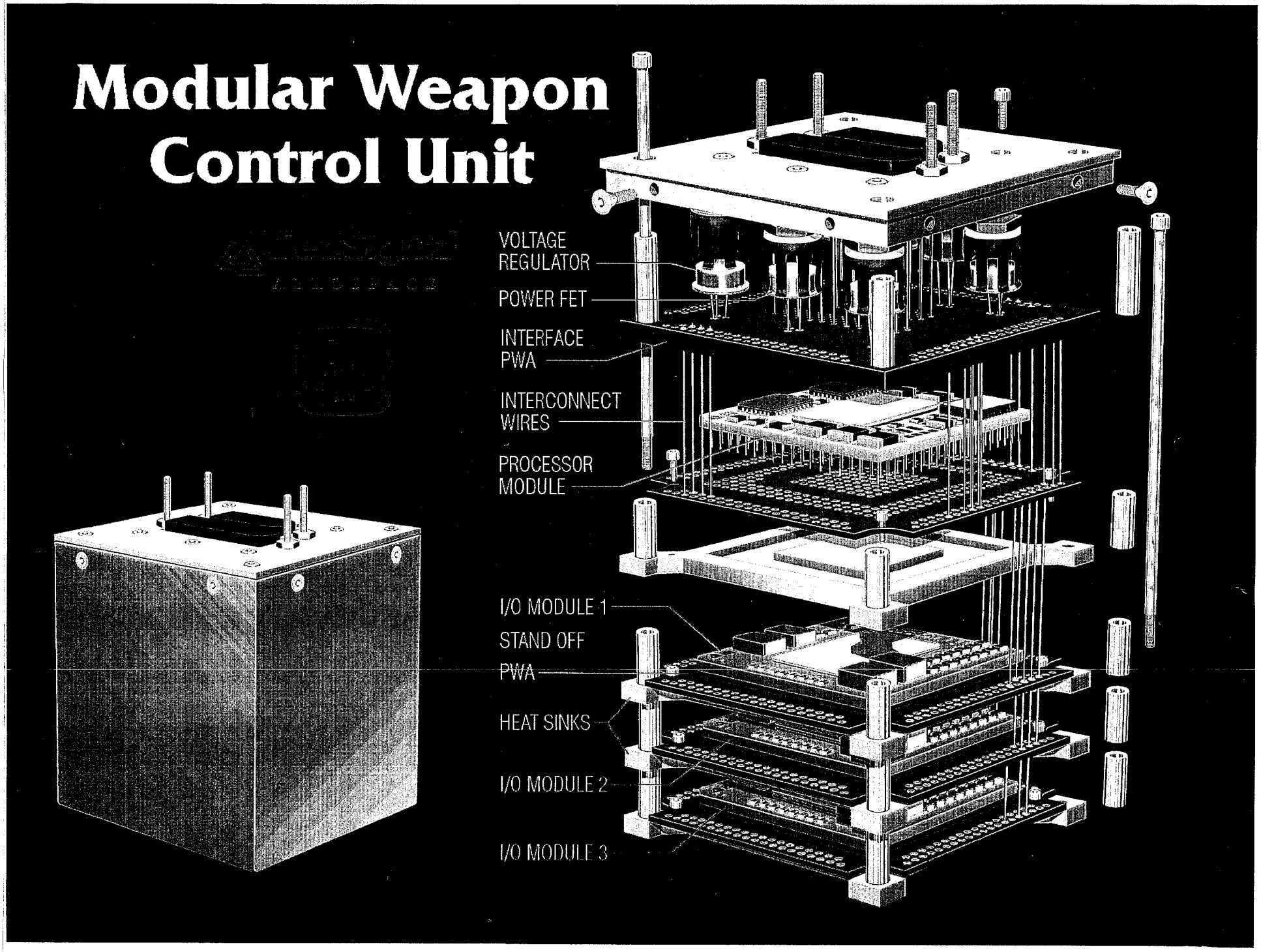
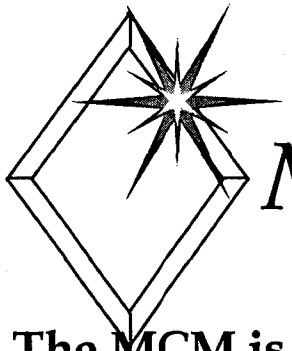


Figure 23. MWCU Concept Drawing 2.



Multichip Module (MCM)

The MCM is a microelectronic assembly composed of standard and custom designed integrated circuits and surface mount components that are attached to a multilayer, high-density, three-dimensional, interconnected substrate. MCM enable more electrical functionality and performance in a smaller volume. Some fundamental advantages of MCM technology are:

- **Increased functionality per unit volume**
- **Increased system speed**
- **Ability to handle integrated circuits with large numbers of I/Os**
- **Increased number of interconnections in a small area**
- **Reduced number of external connections for a given system function**

MCM applications include:

- **Communications**
- **Military/Aerospace**
- **Automotive/Consumer**
- **Industrial and Instrument**
- **Computer/Peripheral**

Figure 24. MWCU Processor Module (PM) Presentation (1 of 6).

MCM Process Flow

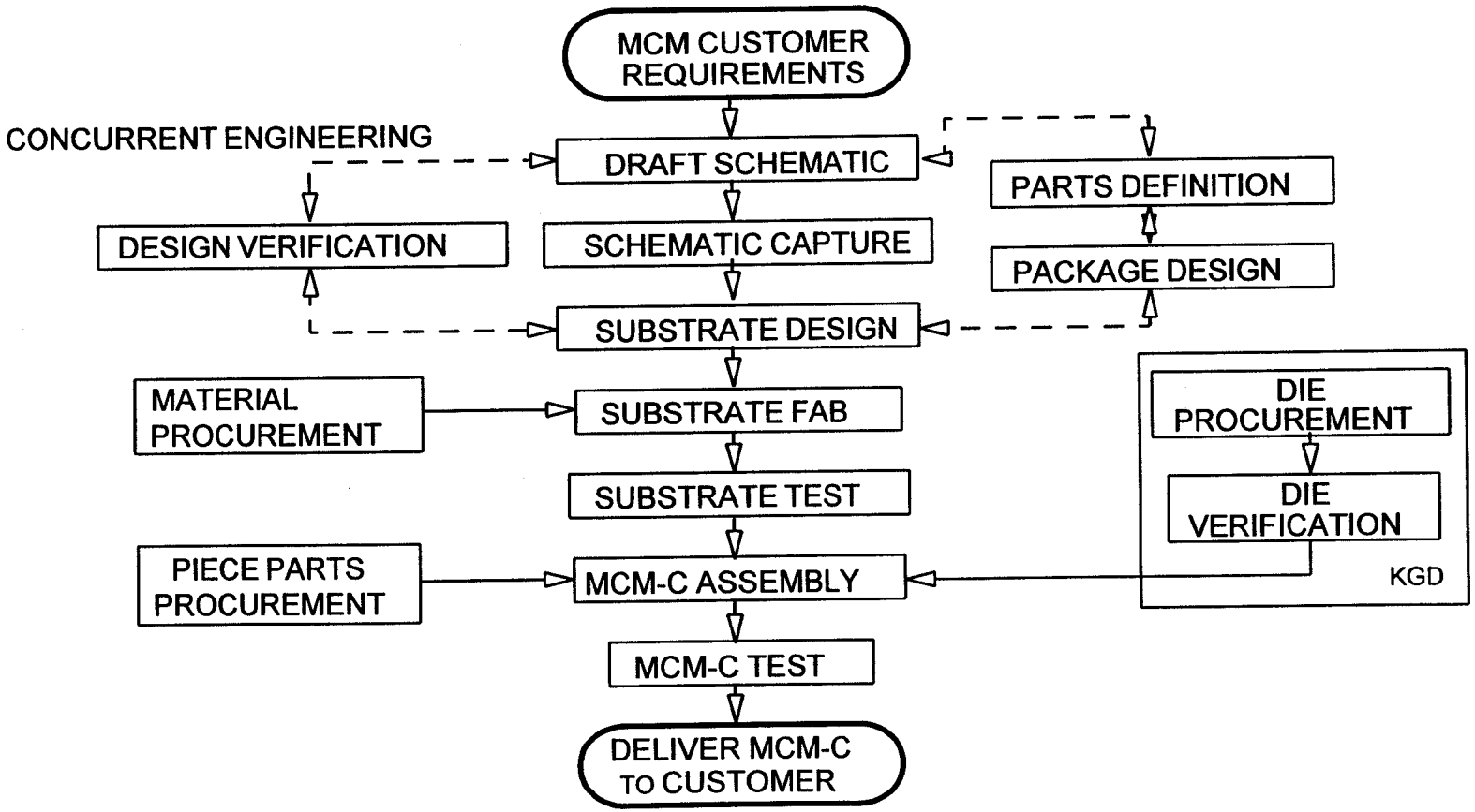
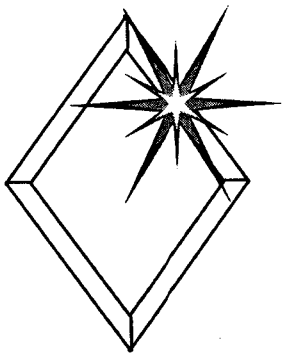


Figure 24. MWCU Processor Module (PM) Presentation (2 of 6).



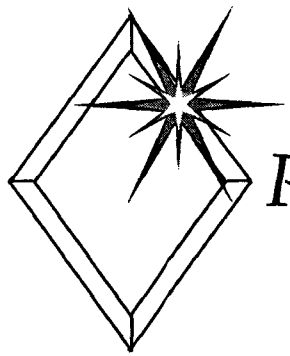
High Density Digital MCM-C Development at KCD

- Develop multichip module (MCM) technology to support the anticipated use of this new technology for weapon upgrades and stockpile improvement designs from the design agencies.

- Prototype MCMs have been selected that are consistent with plans and interests at the design agency, Sandia National Laboratories in New Mexico.

- The small scale production of each MCM focuses on detection and resolution of design, fabrication, and testing problems surrounding the MCM technology.

Figure 24. MWCU Processor Module (PM) Presentation (3 of 6).



Processor Module (PM)

The processor module performs all processing and decision making functions. The module's capabilities include five internal programmable timers, two serial communication channels, one parallel channel, and forty-eight channels of programmable, discrete, digital, input/output lines. A surface mount read only memory (ROM) provides capability to define the module's task.

Processor Module Structure

- **2.0" X 2.0" low temperature cofired substrate**
- **16 layers of ceramic, 118 electrical nets, 1923 electrical vias**
- **Single cavity, 10 ICs, two-tiered wire bondout cavity**
- **Components on a high thermal conducting aluminum nitride subcarrier**
- **7 thick film resistors**
- **26 surface mount components**
- **165 PGA pins, thermal vias**

Figure 24. MWCU Processor Module (PM) Presentation (4 of 6).

Processor Module (PM)

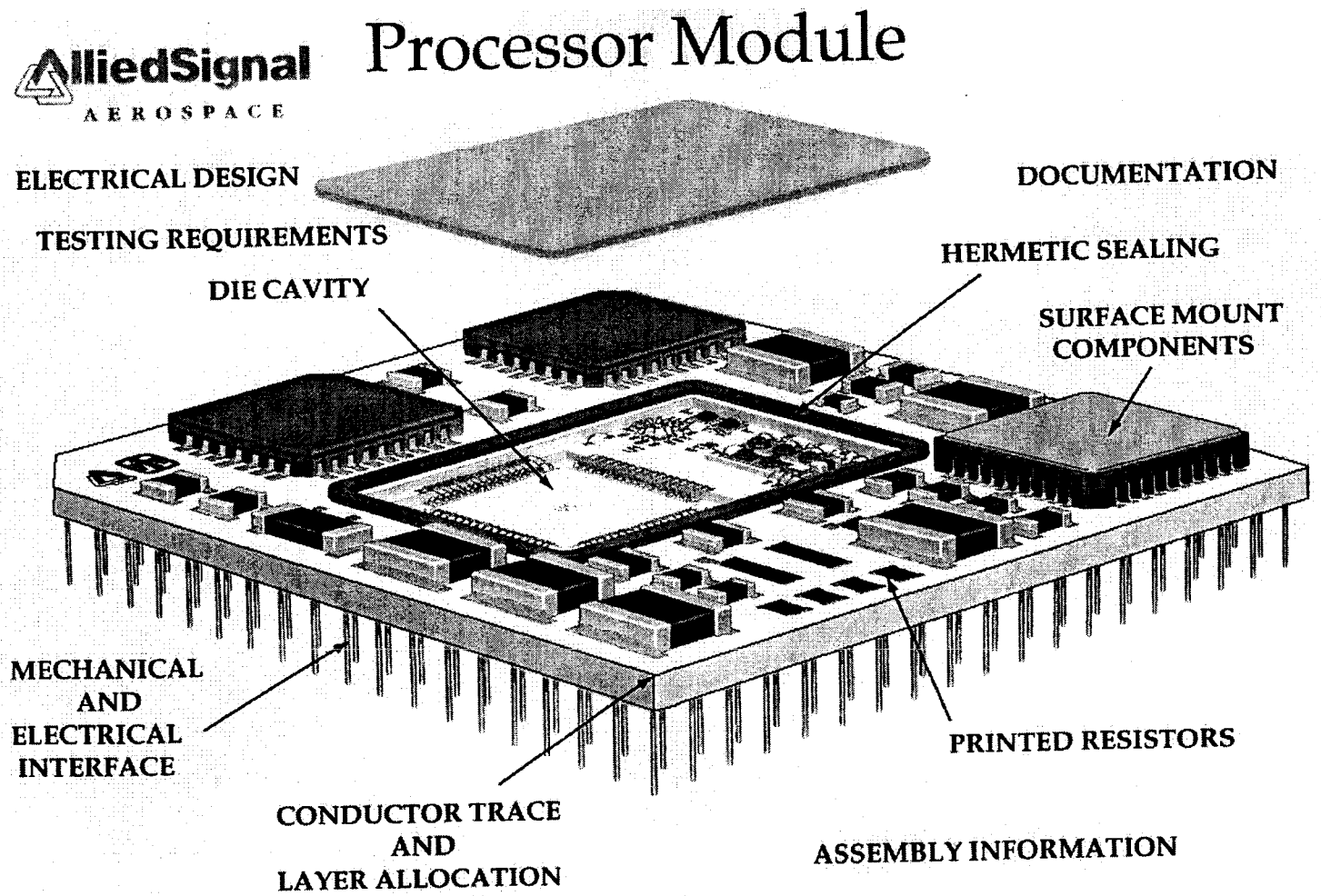


Figure 24. MWCU Processor Module (PM) Presentation (5 of 6).

Processor Module (PM)

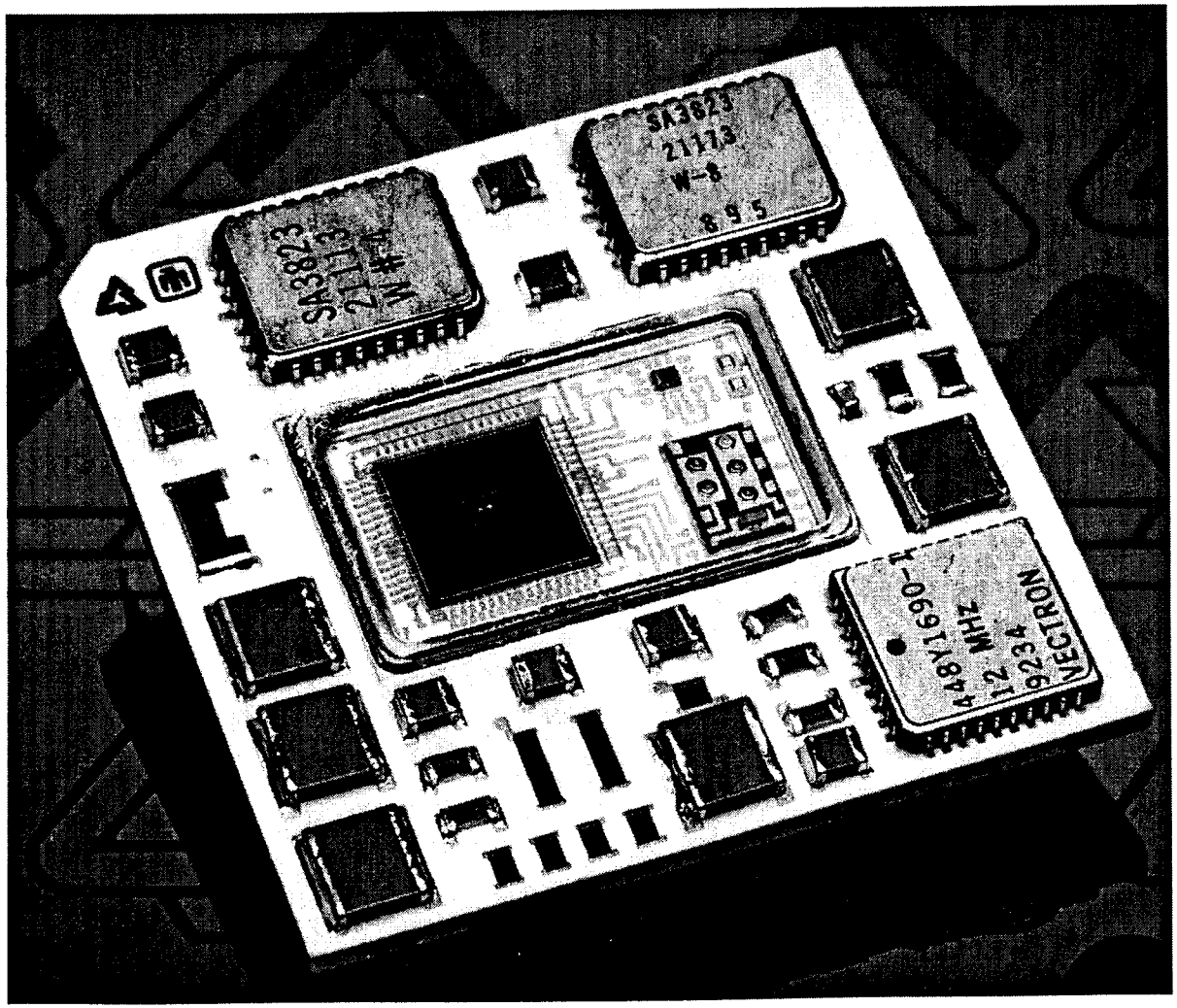
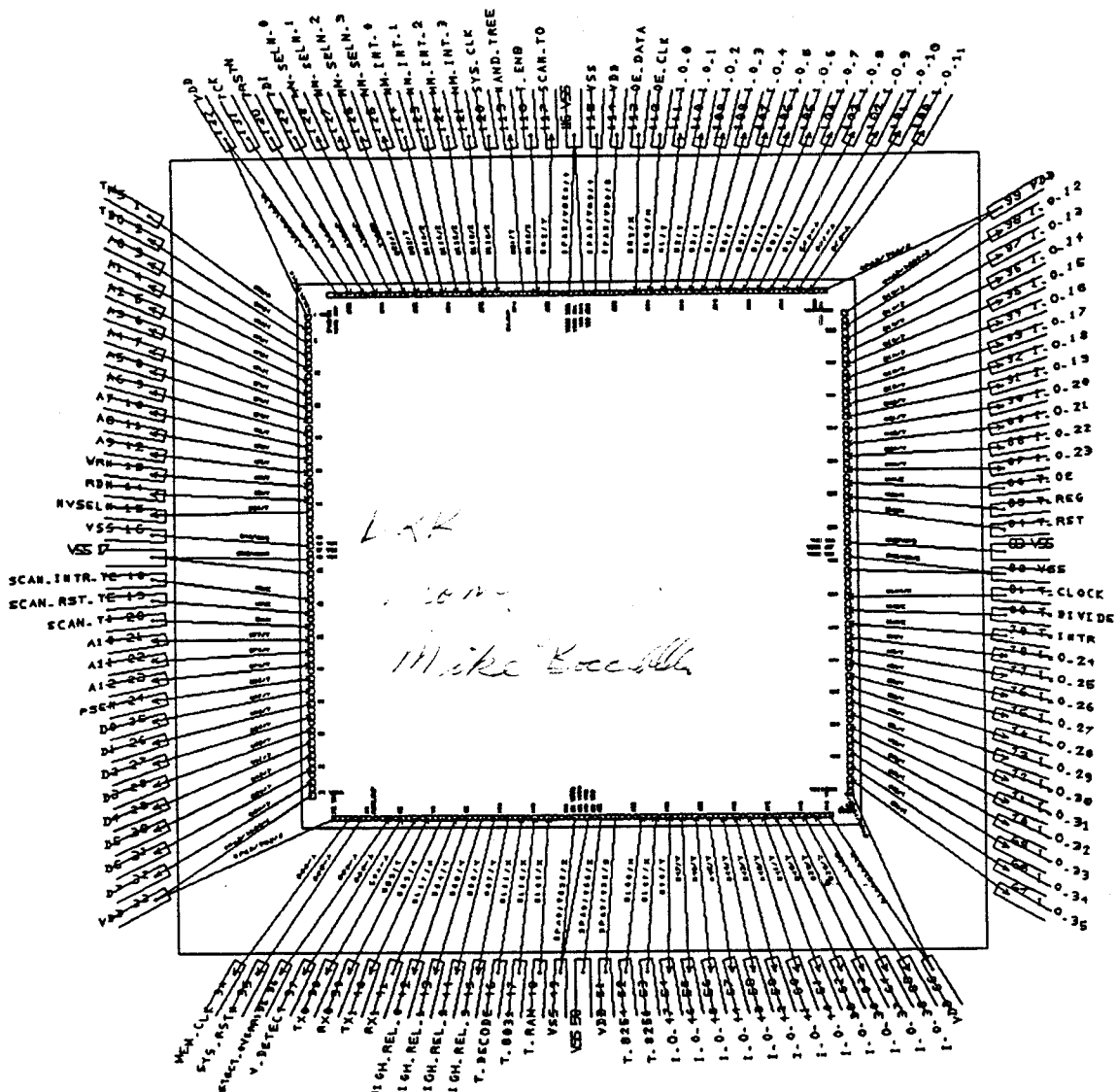


Figure 24. MWCU Processor Module (PM) Presentation (6 of 6).



L1A8087 MWCU FROM BTM

DATE RELEASED MON DEC 7 13:00:56 1992

BDCMD TIME MON DEC 7 10:47:19 1992

DESCRIPTION

132 PGA C/U 0.600 CAVITY

BONDING DIAGRAM NOTEPAD

PACKAGE CODE - FH60

DIE SIZE - 10.500MM X 10.500MM

APPROVALS:

ENG _____ *

PKG _____ *

QA _____

CUST _____

* APPROVALS REQUIRED — WARNINGS/VIOLATIONS EXIST

REQUIRES LOW TEMP PROCESS (360C MAX)

REQUIRES ISOLATED or VSS D/A CAVITY

FOR PLASTIC, USE BOTTLENECK CAPILLARY

10.057	DOC #	PAGE OF

Figure 25. MWCU Processor ASIC Pinout (1 of 4).

```
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*                    BONDING DIAGRAM COMMAND FILE                           *
*                                                                           *
*           PACKAGE CODE: FH60                                              *
*           PACKAGE DESCRIPTION:    132 PGA C/U 0.600 CAVITY                *
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*
*            PIN-NAME            OPTION                    PIN#     PAD#
* * *    1: Place all VSS
*
PLACE         VSS                                          16       36
PLACE         VSS                                          50       115
PLACE         VSS                                          83       188
PLACE         VSS                                          115      258
* * *    2: Place all VSS2
*
PLACE         VSS2                                         17       40
PLACE         VSS2                                         49       111
PLACE         VSS2                                         82       184
PLACE         VSS2                                         116      262
* * *    3: Place all VSS3
*
PLACE         VSS3                                         17       38
PLACE         VSS3                                         49       113
PLACE         VSS3                                         82       186
PLACE         VSS3                                         116      260
* * *    4: Place all VDD
*
PLACE         VDD                                          33       75
PLACE         VDD                                          66       149
PLACE         VDD                                          99       224
PLACE         VDD                                          132      1
PLACE         VDD                                          51       117
PLACE         VDD                                          114      256
* * *    5: Place all VDD3
*
PLACE         VDD3                                         33       74
PLACE         VDD3                                         66       150
PLACE         VDD3                                         99       223
PLACE         VDD3                                         132      297
* * *    6: Place all input and output signals
*
PLACE         MM_INT_0                                     124      281
PLACE         MM_INT_1                                     123      279
PLACE         MM_INT_2                                     122      277
PLACE         MM_INT_3                                     121      275
PLACE         RX0                                          39       89
PLACE         RX1                                          41       93
PLACE         SYS_CLK                                      120      273
PLACE         TCK                                          131      295
PLACE         TDI                                          129      291
PLACE         TMS                                          1        3
PLACE         TRSTN                                        130      293
PLACE         V_DETECT                                     37       85
PLACE         V_DETECT_OVERRIDE                            36       83
PLACE         A0                                           3        7
PLACE         A1                                           4        9
PLACE         A2                                           5        11
PLACE         A3                                           6        13
PLACE         A4                                           7        15
PLACE         A5                                           8        17
PLACE         A6                                           9        19
PLACE         A7                                           10       21
PLACE         A8                                           11       23
PLACE         A9                                           12       25
PLACE         A10                                          21       50
```

Figure 25. MWCU Processor ASIC Pinout (2 of 4).

PLACE	A11	22	52
PLACE	A12	23	54
PLACE	HIGH_REL_0	42	95
PLACE	HIGH_REL_1	43	97
PLACE	HIGH_REL_2	44	99
PLACE	HIGH_REL_3	45	101
PLACE	MEM_CLK	34	77
PLACE	MM_SELN_0	128	289
PLACE	MM_SELN_1	127	287
PLACE	MM_SELN_2	126	285
PLACE	MM_SELN_3	125	283
PLACE	NVSELN	15	31
PLACE	PSEN	24	56
PLACE	RDN	14	29
PLACE	SYS_RSTN	35	79
PLACE	TDO	2	5
PLACE	TX0	38	87
PLACE	TX1	40	91
PLACE	WRN	13	27
PLACE	D0	25	58
PLACE	D1	26	60
PLACE	D2	27	62
PLACE	D3	28	64
PLACE	D4	29	66
PLACE	D5	30	68
PLACE	D6	31	70
PLACE	D7	32	72
PLACE	I_O_0	111	248
PLACE	I_O_1	110	246
PLACE	I_O_2	109	244
PLACE	I_O_3	108	242
PLACE	I_O_4	107	240
PLACE	I_O_5	106	238
PLACE	I_O_6	105	236
PLACE	I_O_7	104	234
PLACE	I_O_8	103	232
PLACE	I_O_9	102	230
PLACE	I_O_10	101	228
PLACE	I_O_11	100	226
PLACE	I_O_12	98	221
PLACE	I_O_13	97	219
PLACE	I_O_14	96	217
PLACE	I_O_15	95	215
PLACE	I_O_16	94	213
PLACE	I_O_17	93	211
PLACE	I_O_18	92	209
PLACE	I_O_19	91	207
PLACE	I_O_20	90	205
PLACE	I_O_21	89	203
PLACE	I_O_22	88	201
PLACE	I_O_23	87	199
PLACE	I_O_24	78	174
PLACE	I_O_25	77	172
PLACE	I_O_26	76	170
PLACE	I_O_27	75	168
PLACE	I_O_28	74	166
PLACE	I_O_29	73	164
PLACE	I_O_30	72	162
PLACE	I_O_31	71	160
PLACE	I_O_32	70	158
PLACE	I_O_33	69	156
PLACE	I_O_34	68	154
PLACE	I_O_35	67	152
PLACE	I_O_36	65	147
PLACE	I_O_37	64	145
PLACE	I_O_38	63	143

Figure 25. MWCU Processor ASIC Pinout (3 of 4).

```
PLACE       I_O_39                                          62      141
PLACE       I_O_40                                          61      139
PLACE       I_O_41                                          60      137
PLACE       I_O_42                                          59      135
PLACE       I_O_43                                          58      133
PLACE       I_O_44                                          57      131
PLACE       I_O_45                                          56      129
PLACE       I_O_46                                          55      127
PLACE       I_O_47                                          54      125
PLACE       T_ENB                                           118     267
PLACE       T_DECODE                                        46      103
PLACE       T_8031                                          47      105
PLACE       T_RAM                                           48      107
PLACE       T_8254                                          52      121
PLACE       T_8251                                          53      123
PLACE       T_INTR                                          79      176
PLACE       T_DIVIDE                                        80      178
PLACE       T_CLOCK                                         81      180
PLACE       T_RST                                           84      193
PLACE       T_REG                                           85      195
PLACE       T_OE                                            86      197
PLACE       OE_CLK                                          112     250
PLACE       OE_DATA                                         113     252
PLACE       SCAN_INTR_TE                                    18      44
PLACE       SCAN_RST_TE                                     19      46
PLACE       SCAN_TI                                         20      48
PLACE       SCAN_TO                                         117     265
PLACE       NAND_TREE                                       119     269
* * *   7: Place all internal pad drivers (high fanout buffers)
*
PLACE       CLK_BUF                                                 271
PLACE       RSTN_BUF                                                81
* * *   8: Replace default save name with new name if desired
*           Do not save the design to the top module name
*
SAVE    8087BD
*
* * *   9: Replace default message with your own personalized message
PLOT    L1A8087 MWCU from BTM
EXIT
```

Figure 25. MWCU Processor ASIC Pinout (4 of 4).

MWCU
Processor Module

AlliedSignal
AEROSPACE

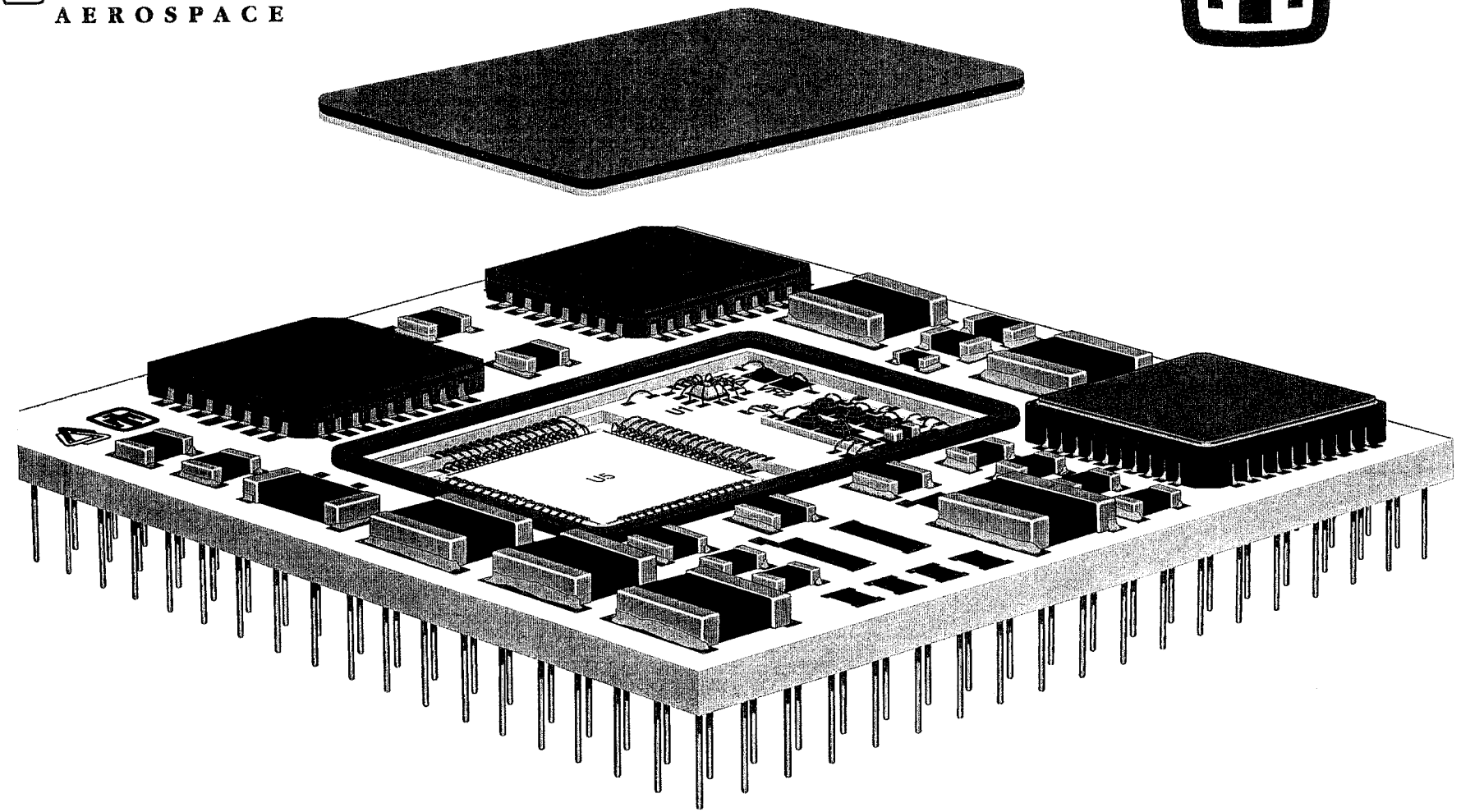


Figure 26. MWCU PM Drawing.

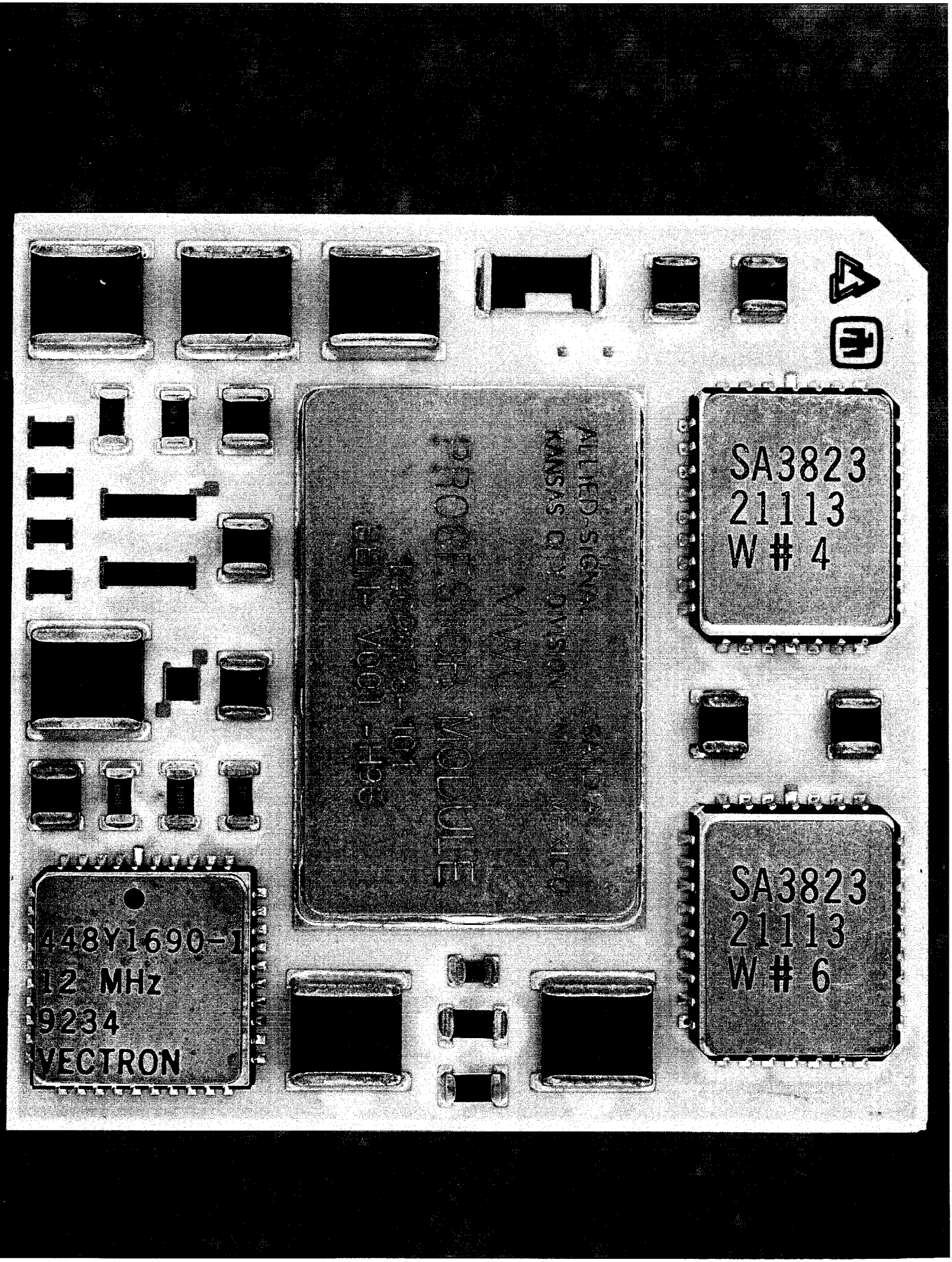


Figure 27. MWCU PM Top Picture.

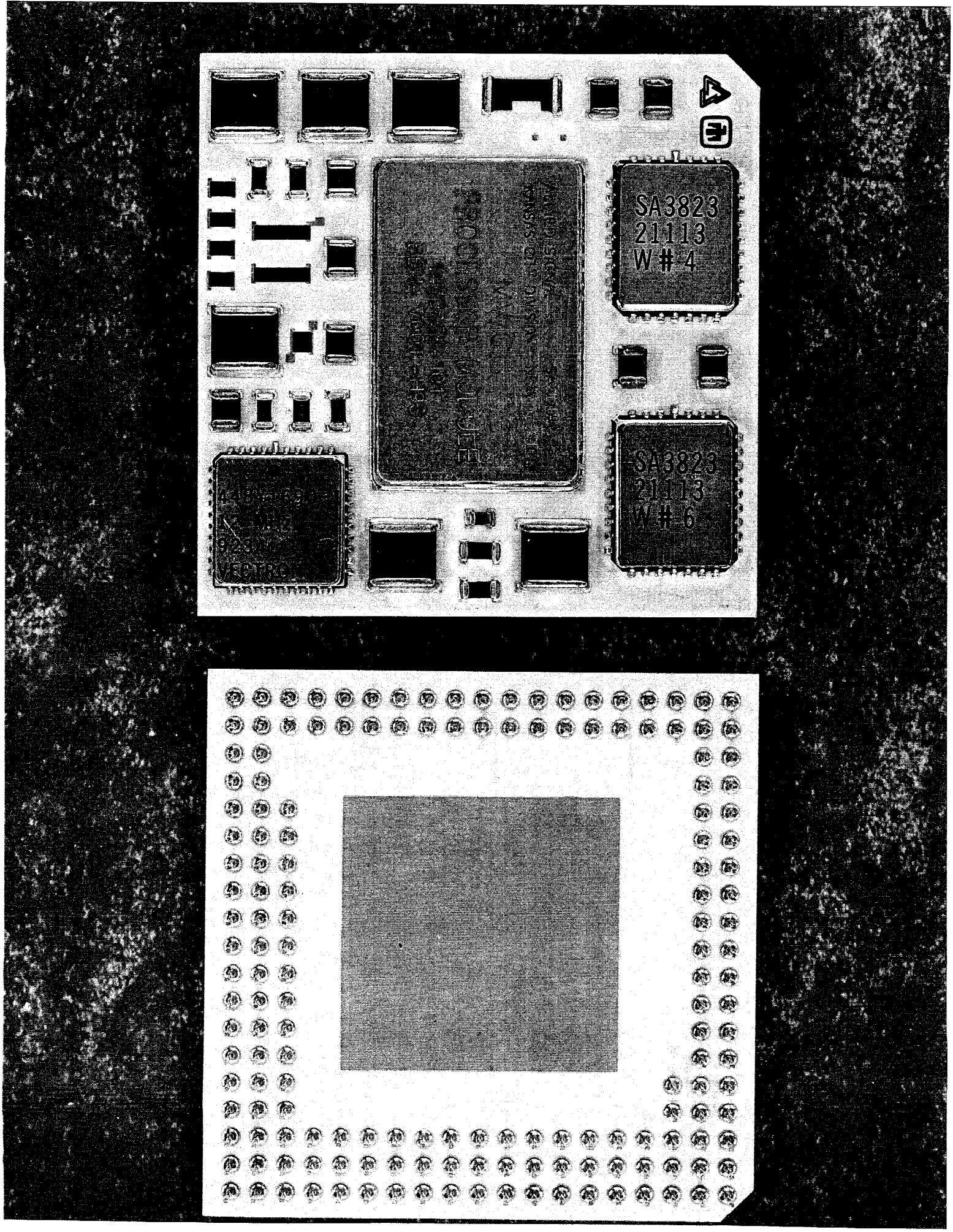


Figure 28. MWCU PM Top/Bottom Picture.

Input/Output Module (IOM)

The input/output (I/O) module will perform input level shifting and signal conditioning for eight lines and provide different output drives for eight lines. Drive capability for the outputs include:

- ✓ **Two, 250 mA steady state lines**
- ✓ **Two, 3.0 A steady state lines**
- ✓ **Four, 5.0 A, 20 msec pulsed lines**

The I/O module has three pull down lines and an analog to digital converter. The processor module provides the control for the I/O module.

Input/Output Module Structure

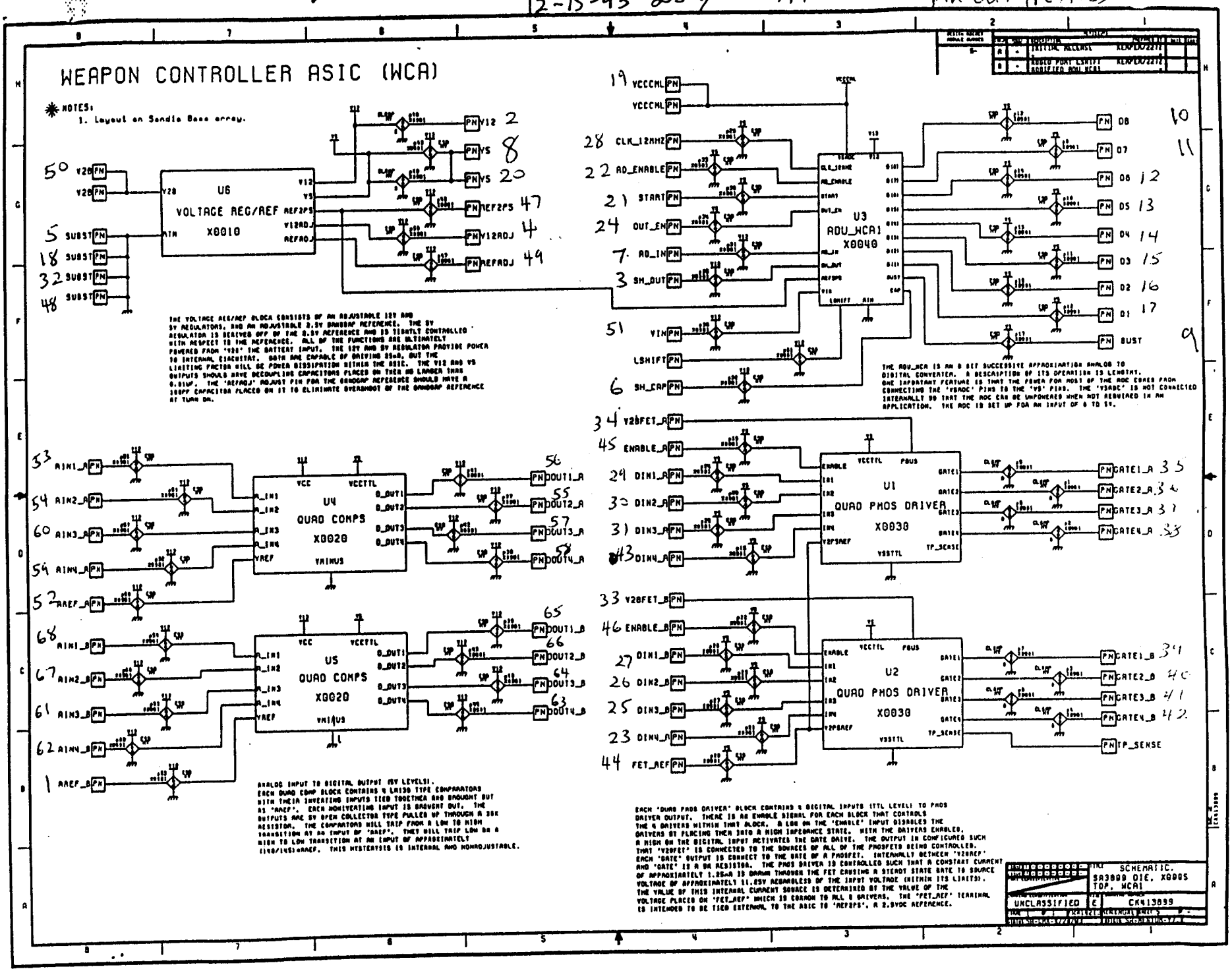
- ° **2.0" X 2.0" low temperature cofired substrate**
- ° **8 layers of ceramic, 91 electrical nets, 902 electrical vias**
- ° **Single cavity, 27 die**
- ° **Components on an aluminum nitride, thin film subcarrier**
- ° **39 surface mount components**
- ° **165 PGA pins, staggered thermal vias**

Figure 29. MWCU Input/Output Module (IOM) Presentation (1 of 3).

Figure 29. MWCU Input/Output Module (IOM) Presentation (2 of 3).

Input/Output Module (IOM)

Figure 29. MWCU Input/Output Module (IOM) Presentation (3 of 3).



Latest version of WCA1 12-15-93 SJL / WCA1

6-28-95 Pin Out (PCAMs)

Figure 30. MWCU IOM ASIC Schematic.

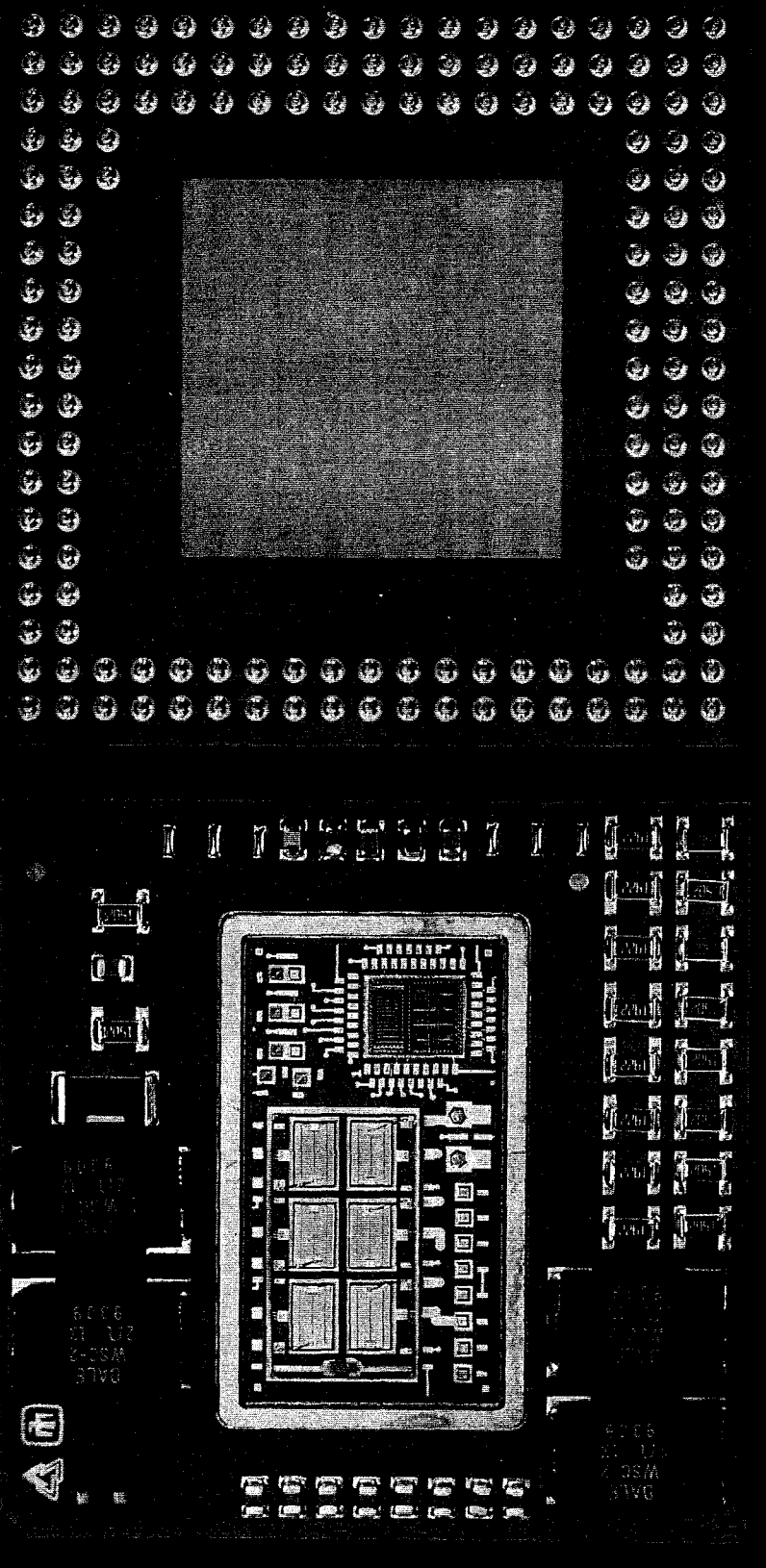


Figure 31. MWCU IOM Top/Bottom Picture.

UNLIMITED RELEASE:

1	MS0537	S. P. Ulibarri, 2314
5	MS0537	G. N. McGovney, 2314
1	MS9018	Central Technical Files, 8940-2
5	MS0899	Technical Library, 4414
2	MS0619	Review & Approval Desk, 12630 For DOE/OSTI